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New device matching strategies for high-precision analog and mixed-signal circuits

by

Tao Zeng

A dissertation submitted to the graduate faculty

in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

Major: Electrical Engineering

Program of Study Committee:
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Iowa State University
Ames, Iowa
2013

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DEDICATION

To my parents

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In 2004, I started my undergraduate study at Iowa State University. Nine years later, I am writing this dissertation for the completion of Ph.D. degree. There are no words to express my feelings for this precious experience, but sadly, the days at Iowa State University is coming to an end. Throughout the years, many people have helped me.

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ABSTRACT

For several decades, technology scaling has brought many orders of magnitude improvements in digital CMOS performance and similar economic benefits to consumers. Feature size is quickly approaching nanometer scale, and the associated large variability imposes grand challenges in achieving reliable and robust operation. This is especially so for high-precision analog and mixed-signal circuits since they have always relied on accurate device matching which will not be available in nanometer CMOS or emerging technologies. This dissertation is aiming to develop design methodologies for overcoming such grand challenges without the conventional matching requirements. The underlining hypothesis is that, from a population of devices with significant variability, correct interconnection and sequencing can produce an effective system level matching that is several orders of magnitude better than the original devices. The optimal solution is non-deterministic polynomial-time hard but a simple ordered element matching strategy based on ordered statistics produces dramatically improved matching. Practical implementation of the new matching strategy is demonstrated on a 15-bit binary-weighted current-steering digital-to-analog converter design in a 130nm CMOS technology. The core area of the chip is less than 0.42mm^2, among which the MSB current source area is well within 0.021mm^2. Measurement results have shown that the differential nonlinearity and integral nonlinearity can be reduced from 9.85LSB and 17.41LSB to 0.34LSB and 0.77LSB, respectively.

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CHAPTER 1

OVERVIEW

1.1 Introduction

For several decades, the semiconductor industry has been relentlessly pushing to decrease the cost-per-function measure of integrated circuits (ICs). The minimum feature size in state-of-the-art digital CMOS process has been in deep submicron for some time and is quickly approaching nanometer scale. In these technology nodes and beyond, significant variability due to process, supply voltage, temperature, and stress (PVTS) variations, impose grand challenges to the design of high performance, reliable, and robust circuits and systems. With emerging materials and devices that may offer an alternative to CMOS, variability is no less.

Achieving high precision and high linearity for analog and mixed-signal circuits and systems in nanometer and emerging technologies is an even greater challenge. This is because most of the important parameters for these circuits such as gain, linearity, signal to noise ratio, and many others, do not benefit from the technology scaling. In fact, they suffer significantly from it. One of the most important process properties from which high precision and high linearity are derived is device matching, be it transistor matching, capacitor matching, or resistor matching. The matching properties of these devices become considerably worse as the technologies continue to advance. Consequently, the performance variability in the circuits that are implemented by these devices will increase dramatically.

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Since device mismatch is so poor in the nanometer and emerging technologies, no traditional methodologies can handle. Solving the matching problem will have incredibly wide impacts as many systems have built-in analog and mixed-signal functions whose performance typically defines the overall system performance. Such systems include audio and video functions in consumer electronics, wireless base stations, and deep-space instrumentations, and many other applications involving both digital and real worlds.

1.2 Dissertation organization

This dissertation is aiming at developing matching strategies to achieve high precision and high linearity in analog and mixed-signal circuits with the presence of large random component variations. The underlining hypothesis is that from a population of elements with significant variability, correct interconnection and sequencing can produce an effective system level matching that is several orders of magnitude better than the original elements. Although the problem of achieving the optimal system level matching can be shown to be non-deterministic polynomial-time (NP) hard, a simple heuristic strategy called ordered element matching (OEM) based on ordered statistics can produce dramatically improved matching. Furthermore, this work will develop practical implementations of the OEM strategy and demonstrate its great matching improvements for a high-resolution current-steering digital-to-analog converter (DAC) in one of the modern CMOS technologies.

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Chapter 2 of this dissertation emphasizes the theoretical background of OEM utilizing results from the area of order statistics. The new theory is motivated by data converter designs which represent a large class of analog and mixed-signal circuits. From thorough statistical analysis, it is proven to be capable of reducing standard deviation of the random mismatch errors by a factor of at least 6.5 in a reasonably sized component population. Meanwhile, an outlier elimination strategy can be incorporated by putting in additional elements to enhance the matching performance. In order to take the maximum benefit offered by OEM, a "binarization" strategy is also proposed, which generates a well matched binary-weighted array from a mismatched unary-weighted array by n−1 OEM iterations in the case of an n-bit structure.

In Chapter 3, a 15-bit binary-weighted current-steering DAC is designed and fabricated in a standard 130nm CMOS technology. The new matching strategies are applied to the 7-bit most-significant-bit (MSB) array, while the 8-bit least-significant-bit (LSB) array is implemented based on the intrinsic accuracy of the fabrication technology. The core area of the chip is less than $0.42mm^2$, among which the MSB current source area is well within $0.021mm^2$. Measurement results have shown that the differential nonlinearity (DNL) and integral nonlinearity (INL) performance can be reduced from 9.85LSB and 17.41LSB to 0.34LSB and 0.77LSB, respectively.

Chapter 4 illustrates the optimal binarization problem which is shown to be NP-hard. Several other heuristic binarization strategies are proposed. By considerations of both practical and computational complexity, OEM binarization features simplicity and efficiency, and it offers the similar matching performance compared to the other

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binarization methods. Meanwhile, in this chapter, we also emphasize how to develop an optimal segmentation for OEM binarization by considering a tradeoff between resource and linearity performance. Based on the tradeoff, multiple versions of optimization problems are formulated. Then, a simple heuristic approach is presented to one of these optimization problems, which synthesizes near-optimal segmentation solutions. The proposed approach can be applied to any data converter designs regardless of implementation details. It can be shown that traditional segmentations do not always guarantee the best tradeoff.

Finally, Chapter 5 concludes this dissertation.

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CHAPTER 2

AN ORDER-STATISTICS BASED MATCHING STRATEGY FOR CIRCUIT COMPONENTS IN DATA CONVERTERS

2.1 Introduction

Data converters are the interfaces for information flowing between the digital and real worlds. They play crucial roles in many electronic circuits and systems today. Analog-to-digital converters (ADCs) covert an analog voltage or current into digital domain for further digital signal processing, whereas digital-to-analog converters (DACs) convert digital information into analog domain as representations of voltage, current, or electric charge to carry out real-world functions. Many ADCs [1]-[10] and DACs [11]-[20] rely on matched circuit components such as transistors, resistors, or capacitors to perform their data conversion tasks. However, the IC fabrication technology invariably produces imperfectly matched circuit components. The imperfections lead to component parameters deviating from their designed values. The resulting errors contain a significant random part which is determined by the inherent matching properties of the fabrication process, and they are often termed as random mismatch. As IC technology continues to advance, motivated by Moore's law, random mismatch becomes significantly worse due to shrink of device size and supply voltage [21]-[23]. Since it causes electrical property variations of the fabricated elements which result variability in circuit properties, random mismatch is considered as one of the

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major sources of error that degrade linearity performance and parametric yield of many analog and mixed-signal circuits and systems, especially of data converters.

The variations in component parameters caused by random mismatch are random in nature, and thus they are modeled as random variables with mean of zero and standard deviation related to the physical area of matching-critical components [24]-[29]. In general, a factor of four augmentation in area corresponds to a factor of two reduction in standard deviation of the mismatch errors. Therefore, 1-bit linearity enhancement will lead to a quadruple of circuit area. Nevertheless, the maximum allowed area is limited by the available die size as growing number of circuits and systems are integrated into a single chip. Additionally, large device dimensions deteriorate parasitic capacitance effects which limit the achievable speed of data converters and in some cases increase the power consumptions [10], [30].

Besides increasing the area, many other techniques can be applied to compensate random mismatch errors in the matching-critical components for data converters. They can be divided into four categories, i.e., trimming, calibration, switching-sequence adjustment, and dynamic element matching (DEM). Each category is briefly discussed in the following paragraphs.

Trimming compensates the random mismatch errors by regulating the component parameters at the wafer stage. It requires accurate test equipments to continuously measure and compare trimmed parameters with their nominal values. There are mainly two types of trimming. One is to change the physical dimensions of the circuit elements by applying laser beams [11], [19], whereas the other one is to connect/disconnect an

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array of binary-weighted small elements using fuses or MOS switches [29]. Both forms of trimming can be cost-ineffective in test time and equipments, and the achieved accuracy does not account for temperature and aging effects [31].

Calibration alleviates the random mismatch effect by feeding back either digital or analog correction signals to the data converters' input or output after measuring errors based on an available reference. Calibration can be treated as an improved version of trimming since it characterizes errors on chip or board and continuously corrects them over different time and environments. Some calibration techniques have to be performed at circuit power-up or stand-by phase [11], [16], [17], while some can be done in background without any interference to the normal operation [5]-[7], [9], [10]. Yet, the obtained accuracy level is limited by the resolution and accuracy of error measurement circuits and correction signals.

Switching-sequence adjustment is commonly used in layout designs to compensate the systematic gradient errors [13], [14], [29]. In recent publications [18], [20], this method has been extended to compensate random mismatch errors in the data converters. It improves linearity performance by changing component switching sequence according to the parameter orders. That is to place an element having smaller parameter in neighbor with the one having larger parameter. However, this approach only improves the integral nonlinearity (INL), and the differential nonlinearity (DNL) remains unchanged which greatly limits the matching efficiency.

DEM is another popular solution to the random mismatch errors for matching–critical components. It dynamically changes the positions of mismatched elements at

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different time so that the equivalent component at each position is nearly matched on a time average. Some examples of this technique can be found in [2], [3], [15], [32]-[34]. Among all of these, the popular algorithms are butterfly randomization [32], individual level averaging [33], and data weighted averaging [15], [34]. Unlike the static random mismatch compensation techniques, DEM translates mismatch errors into noise. However, the translated noise is only partially shaped where the in-band residuals could possibly affect the data converters' signal-to-noise ratio (SNR) [35]. Furthermore, the output will be inaccurate at one time instant since DEM only guarantees matching on average, and thereby it cannot be implemented in some applications.

In this chapter, we introduce a novel random mismatch compensation theory called ordered element matching (OEM), which does not fall into any of the four categories mentioned above. It sorts the circuit components based on their parameter magnitudes, and then pairs and sums the complimentary ordered components. By doing so, it creates a new sample population with twice larger in magnitude but much smaller variations than those of the original sample population. Since random mismatch errors are modeled as random variables with certain statistical characteristics, a statistical analysis is performed to validate this theory. The statistics of the sorted and summed random variables can be obtained based on the theory of order statistics. The variation reduction factors are calculated by comparing the standard deviations between statistics of original and summed random variables.

The OEM theory is derived based on the definition of quasi-midranges in the subject of order statistics, where they are the half of the sum of complimentary ordered

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samples in a population [36]. Quasi-midranges sometimes serve as a fast estimation for the mean of a sample population; however, they are known to be sensitive to the outliers of parent distributions [36], [37]. This knowledge also holds for the OEM theory, and the standard deviations of those outlying summed random variables are shown to be substantially larger than the others in statistical analysis. Then, an outlier elimination strategy is proposed to omit a certain number of outlying elements in the original samples and thereby further reduces the parameter variations. More importantly, it considerably improves the DNL performance in a reasonably sized component population.

Based upon these, we develop a new matching technique called complete-folding, which can dramatically reduce both DNL and INL by selectively regrouping circuit elements according to their parameter orders and eventually transforming a unary-weighted array into a binary-weighted array. It has been demonstrated in [38] that this technique has a significant impact on linearity performance and parametric yield in a current-steering DAC design. In this work, statistical simulations are performed by using the complete-folding technique to justify the results obtained from the statistical analysis.

This chapter is organized as follows. Section 2.2 introduces the OEM theory in details along with statistical formulations using the theory of order statistics. Section 2.3 addresses the outlier elimination strategy and the ensuing standard deviation reduction based on statistical analysis. In Section 2.4, the basic functionality of complete-folding technique is illustrated, and meanwhile the circuit realization is briefly discussed.

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Section 2.5 presents the matching accuracy improvement in a current source array when both complete-folding and outlier elimination are applied. Comparisons are also made among the competing static random mismatch compensation techniques. Significant linearity enhancement and design cost reduction are observed. Finally, the chapter is summarized in Section 2.6.

2.2 Ordered element matching

Random mismatch errors in the matching-critical circuit components can severely degrade linearity performance and parametric yield of many data converters, because they cause random variations in the component parameters that lead to unpredictable circuit performance. The OEM theory is aiming at creating a new component population with significantly reduced variations according to the original component parameter orders.

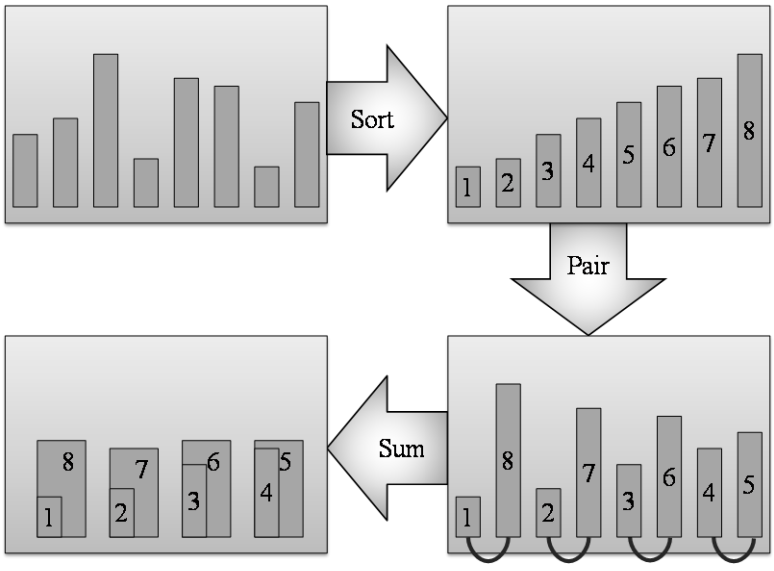

Figure 2.1 The OEM procedure for a unary-weighted resistor array with sample size of 8

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To facilitate the understanding of this new theory, Figure 2.1 illustrates the matching process for a unary-weighted resistor array with sample size of 8. The rectangles in the figure denotes for the resistance values with random variations. The first step is to sort these resistors by their resistance values in the ascending order. All resistors are numbered from 1, 2 … 8 with their respective resistance. The second step is to pair the complimentary ordered resistors into one group. A series of paired resistors are organized as (1, 8), (2, 7), (3, 6), and (4, 5). The final step is to sum the two resistors within each pair and generate a new array of resistors with sample size of 4. The new resistors have resistance values that are twice as large as those in the original array, but their resistance variations are reduced considerably.

This theory is also applicable to improve matching performance in the array of transistors or capacitors where the same procedure can be followed. In those cases, the rectangles in the figure would denote for drain currents and capacitance values, respectively.

2.2.1 Statistical formulation

In order to quantify the amount of variation reduction by OEM, a statistical analysis is performed. Here, the random variations in the component parameters are modeled by a set of Gaussian distributed random variables. Gaussian distribution is used because:: (a) most engineers are more familiar with Gaussian distribution; (b) Gaussian distribution is a good approximation for any random variables affected by a large number of intrinsic random variations, due to the central limit theorem, (c) any other distributions can be approximated by Gaussian distribution if the mean is several

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standard deviations away from the distribution boundaries [39]. However, it should be pointed out that the following statistical analysis can be applied to any distributions, which indicates the OEM theory is even capable of compensating non-Gaussian mismatch errors.

Considering the general cases, we take sample size of the original unary-weighted component array as 2n, where n is an integer number greater than 0. We will prove later that the variation reduction varies from population size selections. It should be also noticed random mismatch is the only considered source of error in this work. All other nonidealities in the matching-critical components such as gradient errors are assumed to be managed by the existing layout strategies [29].

Then, the parameter magnitude for each original circuit component can be expressed as:

$$X_i = \mu + Y_i,\ 1 \le i \le 2n, \tag{2.1}$$

where μ is the nominal parameter value, and X_i and Y_i are the real parameter value and random mismatch error for the ith component, respectively. Random variables Y_i are assumed to be statistically independent and identically distributed (i.i.d.), and they follow Gaussian distribution with mean of 0 and standard deviation of σ, i.e., $Y_i \sim N(0, \sigma^2)$. On the other hand, random variables X_i are also i.i.d. and follow Gaussian distribution with mean of μ and standard deviation of σ, i.e., $X_i \sim N(\mu, \sigma^2)$.

Our objective is to show the random variations can be significantly reduced by applying the OEM theory. To simplify the latter analysis, random variables X_i are transformed into the standard Gaussian distribution according to:

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$$Z_i = \frac{X_i - \mu}{\sigma} \sim N(0,1). \tag{2.2}$$

Z_i can be treated as normalized mismatch errors from the nominal value μ, and their statistical characteristics can be described by the probability density function (PDF) and cumulative distribution function (CDF), i.e., $f_Z(z)$ and $F_Z(z)$, where

$$f_Z(z) = \frac{1}{\sqrt{2\pi}} \exp\left(-\frac{z^2}{2}\right), \quad -\infty < z < \infty, \tag{2.3}$$

$$F_Z(z) = \int_{-\infty}^{z} f_Z(t)\,dt = \frac{1}{2}\left[1 + \mathrm{erf}\left(\frac{z}{\sqrt{2}}\right)\right]. \tag{2.4}$$

In the following analysis, we apply the OEM procedure to random variables Z_i, where they are sorted, paired and summed. The sorting step creates a series of ordered random variables, and the pairing and summing steps generate new random variables with sample size of n based on those ordered ones. The variation reduction factors are obtained by comparing the standard deviations between the original and summed random variables.

2.2.2 Statistics of ordered components

The first step of OEM is to rank the circuit components in the ascending order according to their parameter values. This is equivalent as sorting the random variables Z_i. Suppose Z_1, Z_2 … Z_{2n} are sorted in order of magnitude, and they are written as $Z_{(1;2n)} \le Z_{(2;2n)} \le \ldots \le Z_{(2n;2n)}$, then $Z_{(i;2n)}$ is called the ith order statistic [36].

To study the statistical characteristics of these ordered random variables $Z_{(i;2n)}$, their PDFs and CDFs can be derived based on the theory of order statistics [40]:

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$$f_{Z_{(i;2n)}}(z) = \frac{(2n)!}{(i-1)!(2n-i)!} \cdot \left[F_Z(z)\right]^{i-1} \cdot \left[1-F_Z(z)\right]^{2n-i} \cdot f_Z(z), \quad -\infty < z < \infty, \tag{2.5}$$

$$F_{Z_{(i;2n)}}(z) = \sum_{i}^{2n} \frac{(2n)!}{i!(2n-i)!} \cdot \left[F_Z(z)\right]^{i} \cdot \left[1-F_Z(z)\right]^{2n-i}, \tag{2.6}$$

where $f_Z(z)$ and $F_Z(z)$ have the forms of (2.3) and (2.4), respectively. It is noted that the distribution functions for the ordered random variables are different from each other.

For the ith order statistic $Z_{(i;2n)}$, the expected value $\mu_{(i;2n)}$ and variance $\sigma^2_{(i;2n)}$ can be obtained by computing the corresponding moments as formulated in [40]:

$$EZ^r_{(i;2n)} = \int_{-\infty}^{\infty} z^r f_{Z_{(i;2n)}}(z)\, dz, \tag{2.7}$$

$$\mu_{(i;2n)} = EZ_{(i;2n)}, \tag{2.8}$$

$$\sigma^2_{(i;2n)} = Var\left(Z_{(i;2n)}\right) = EZ^2_{(i;2n)} - \left(EZ_{(i;2n)}\right)^2, \tag{2.9}$$

where r is an integer number greater than 0. It should be noticed the ordered random variables are no longer i.i.d.. Instead, they become correlated after the sorting process. The covariance of the ith and jth order statistics ($Z_{(i;2n)}$ and $Z_{(j;2n)}$) is denoted as $\sigma_{(i,\, j;2n)}$, where

$$\begin{aligned} \sigma_{(i,j;2n)} &= Cov\left(Z_{(i;2n)}, Z_{(j;2n)}\right) \\ &= E\left[\left(Z_{(i;2n)} - \mu_{(i;2n)}\right) \cdot \left(Z_{(j;2n)} - \mu_{(j;2n)}\right)\right], \\ & 1 \le i \le 2n,\ 1 \le j \le 2n. \end{aligned} \tag{2.10}$$

Since the original population follows standard Gaussian distribution, we can derive two moment identities from (2.7), (2.8) and (2.9). They are given below:

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$$\mu_{(i;2n)} = -\mu_{(2n-i+1;2n)}, \tag{2.11}$$

$$\sigma^2_{(i;2n)} = \sigma^2_{(2n-i+1;2n)}. \tag{2.12}$$

The details of derivations can be found in [36] and [40]. Equation (2.11) indicates the expected values of the complementary order statistics ($Z_{(i;2n)}$ and $Z_{(2n-i+1;2n)}$) have the same magnitude but with opposite signs. Equivalently, they are symmetric at the mean value of original population, i.e., 0. On the other hand, according to (2.12), the variance should be the same for the complementary order statistics. Both equations will be used for the statistical analysis when performing the pairing and summing steps.

2.2.3 Statistics of sum of complementary ordered components

The next steps of OEM are to pair and sum the complementary ordered components and generate a new population with sample size of n. This process can be viewed as the error compensation phase and it is as equivalent as adding the complementary order statistics from population $Z_{(1;2n)}$, $Z_{(2;2n)}$ … $Z_{(2n;2n)}$ in our analysis. The obtained new sample population is represented as M_1, M_2 … M_n, where

$$M_k = Z_{(k;2n)} + Z_{(2n-k+1;2n)},\ 1 \le k \le n. \tag{2.13}$$

M_k corresponds to the sum of the kth complementary order statistics. For example, M_1 represents the sum of minimum and maximum ($Z_{(1;2n)}$ and $Z_{(2n;2n)}$) in the original sample population. In addition, the sample size of the new population M_k is reduced to n because of the pairing step.

Intuitively, if we are adding the smaller and larger ordered values in a sample population, the sum tends to be twice as large as the population's mean value. In our

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analysis, the sum will approach to 0, because the mean is normalized to 0. To provide the theoretical justification, we have to examine the statistical characteristics of the new random variables M_k by obtaining their PDFs and CDFs.

The first step is to find the joint PDF of the complementary order statistics, which can be derived from the joint PDF of two order statistics given in [36]:

$$\begin{aligned} f_{Z_{(k;2n)},Z_{(2n-k+1;2n)}}\left(z_{(k;2n)},z_{(2n-k+1;2n)}\right) &= \frac{(2n)!}{\left[(k-1)!\right]^2(2n-2k)!} \\ &\cdot\left[F_Z\left(z_{(k;2n)}\right)\left(1-F_Z\left(z_{(2n-k+1;2n)}\right)\right)\right]^{k-1} \\ &\cdot\left[F_Z\left(z_{(2n-k+1;2n)}\right)-F_Z\left(z_{(k;2n)}\right)\right]^{2n-2k} \\ &\cdot f_Z\left(z_{(k;2n)}\right)\cdot f_Z\left(z_{(2n-k+1;2n)}\right), \\ &-\infty < z_{(k;2n)} \le z_{(2n-k+1;2n)} < \infty, \end{aligned} \tag{2.14}$$

where $f_Z(z)$ and $F_Z(z)$ are given by (2.3) and (2.4), respectively. From (2.13), we have:

$$z_{(2n-k+1;2n)} = m_k - z_{(k;2n)}. \tag{2.15}$$

Followed by this, the joint PDF of M_k and $Z_{(k;2n)}$ can be derived by substituting $z_{(2n-k+1;2n)}$ in (2.14) with (2.15) as shown below:

$$\begin{aligned} f_{M_k,Z_{(k;2n)}}\left(m_k,z_{(k;2n)}\right) &= \frac{(2n)!}{\left[(k-1)!\right]^2(2n-2k)!} \\ &\cdot\left[F_Z\left(z_{(k;2n)}\right)\left(1-F_Z\left(m_k-z_{(k;2n)}\right)\right)\right]^{k-1} \\ &\cdot\left[F_Z\left(m_k-z_{(k;2n)}\right)-F_Z\left(z_{(k;2n)}\right)\right]^{2n-2k} \\ &\cdot f_Z\left(z_{(k;2n)}\right)\cdot f_Z\left(m_k-z_{(k;2n)}\right), \\ &-\infty < z_{(k;2n)} \le \frac{m_k}{2} < \infty. \end{aligned} \tag{2.16}$$

The marginal PDF of M_k is obtained by integrating out (2.16) over $z_{(k;2n)}$:

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$$f_{M_k}(m_k) = \int_{-\infty}^{\frac{m_k}{2}} f_{M_k, Z_{(k;2n)}}\left(m_k, z_{(k;2n)}\right) dz_{(k;2n)}, \quad -\infty < m_k < \infty. \tag{2.17}$$

The CDF of M_k can be computed as:

$$F_{M_k}(m_k) = \int_{-\infty}^{m_k} f_{M_k}(t)\, dt. \tag{2.18}$$

From the derivations above, M_k will have different distribution functions if k and 2n are assigned for different values. Consequently, the standard deviations of these random variables will also be different. Then, when applying the OEM theory, the efficiency of the variation reduction will vary, depending on the order ranks and the original sample population size. The impact of these factors will be thoroughly addressed in the next subsection.

The expected value μ_k and variance σ^2_k of M_k are calculated by their corresponding moments as follows:

$$EM_k^r = \int_{-\infty}^{\infty} m_k{}^r f_{M_k}(m_k)\, dm_k, \tag{2.19}$$

$$\mu_k = EM_k, \tag{2.20}$$

$$\sigma_k^2 = Var(M_k) = EM_k^2 - (EM_k)^2. \tag{2.21}$$

A direct way to obtain μ_k and σ^2_k is to combine (2.10), (2.11), (2.12), (2.13), (2.20), and (2.21) as illustrated below:

$$\begin{aligned} \mu_k &= EM_k = E\left(Z_{(k;2n)} + Z_{(2n-k+1;2n)}\right) \\ &= \mu_{(k;2n)} + \mu_{(2n-k+1;2n)} \\ &= 0, \end{aligned} \tag{2.22}$$

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$$\begin{aligned}\sigma_k^2 &= Var(M_k) = Var\left(Z_{(k;2n)} + Z_{(2n-k+1;2n)}\right) \\ &= \sigma^2_{(k;2n)} + \sigma^2_{(2n-k+1;2n)} + 2\sigma_{(k,2n-k+1;2n)} \\ &= 2\left(\sigma^2_{(k;2n)} + \sigma_{(k,2n-k+1;2n)}\right).\end{aligned} \tag{2.23}$$

Not surprisingly, all random variables M_k have expected value of 0. This is a very important observation, because it indicates the mismatch errors in the normalized sample population Z will be cancelled out by OEM. The same effect will also happen for mismatch errors in the original sample population X. Yet, the expected values μ_k' will be different from (2.22), and they should be twice as large as the nominal parameter value μ. This can be derived based on (2.2) as follows:

$$\begin{aligned}\mu_k' &= E\left(X_{(k;2n)} + X_{(2n-k+1;2n)}\right) \\ &= E\left(\left(\mu + \sigma Z_{(k;2n)}\right) + \left(\mu + \sigma Z_{(2n-k+1;2n)}\right)\right) \\ &= 2\mu + \sigma\left(\mu_{(k;2n)} + \mu_{(2n-k+1;2n)}\right) \\ &= 2\mu.\end{aligned} \tag{2.24}$$

However, random mismatch errors cannot be completely compensated by OEM in a finite sample population. The variance of the residual errors is governed by (2.23). For the later analysis, we will use this knowledge to show the significant standard deviation improvement factors.

2.2.4 Standard deviation reduction calculation

The variation reduction factors can be obtained by comparing the standard deviations between random variables Z_i and M_k. However, in order to have a fair comparison, we need to modify the random variables M_k by multiplying a factor of 0.5.

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This is because the parameter magnitudes in the new sample population after OEM are actually doubled comparing to its original sample population as shown in (2.24). This should be taken into account in the standard deviation analysis even though the standard Gaussian transformation makes the doubling effect undetectable in the expected value analysis. The standard deviations of $0.5M_k$ can be obtained by:

$$\sqrt{Var\left(0.5M_k\right)} = 0.5\sqrt{Var\left(M_k\right)} = 0.5\sigma_k. \tag{2.25}$$

The standard deviations of random variables Z_i will always be unity since they follow standard Gaussian distribution. Here, we can calculate the variation reduction factors A_k by taking the ratio of standard deviations of Z_i to standard deviations of $0.5M_k$, i.e.:

$$A_k = \frac{1}{0.5\sigma_k}. \tag{2.26}$$

As mentioned previously, the standard deviations of M_k varies according to the order ranks (k) and the original sample population size (2n). Therefore, we pick different 2n values to investigate the impact on the variation reduction. Here, 2n is set to be 8, 16, 32, 64, 128, 256, and 512. From (2.21), (2.23) and (2.25), we calculate the standard deviations of $0.5M_k$ for different population sizes and order ranks. The results are plotted and compared in Figure 2.2. It is observed the new population size after OEM is halved in each case, and the standard deviations decrease as the original population size increases. When given a fixed sample population, the standard deviation first drops off as increasing the k values and then slightly bounces back once it reaches the minimum. The rebound near "n" is due to the fact that, in any random population, the number of

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components greater than the mean (positive errors) is inevitably different from the number of components less than the mean (negative errors), and therefore near "n" two components with the same error signs are added while a little before "n" two components with opposite error signs are added. More details on this issue can be found in [37], [40], [41], and [42]. The value of k that minimizes the standard deviations is roughly given by the ratio [40]:

$$\frac{k}{2n} \approx 0.2702. \tag{2.27}$$

The variation reduction factors for each sample population can be obtained by (2.26). Since the quantity A_k varies with k, we shall take its average value as the variation reduction in a given sample population. The obtained results are summarized in Table 2.1. It is noticed the standard deviations of random mismatch errors are reduced significantly. To be quantitative, the variation reduction factor is more than 6.5 for a sample population size greater than 64. In addition, the reduction factor keeps growing with the increase of sample sizes, which indicates the OEM theory is more effective in a large sample population.

On the other hand, it is shown in Figure 2.2 that the standard deviations of $0.5M_k$ in the lower ranks (small k values) are quite large compared to the others in a given sample population. They also have much less reduction when the sample size grows. As a result, these low ranked samples in population M_k limit the overall standard deviation reduction factors. If a certain number of such samples can be excluded from the population, a better reduction can be achieved. In the following section, we will focus on outlier elimination strategy and its related statistical analysis.

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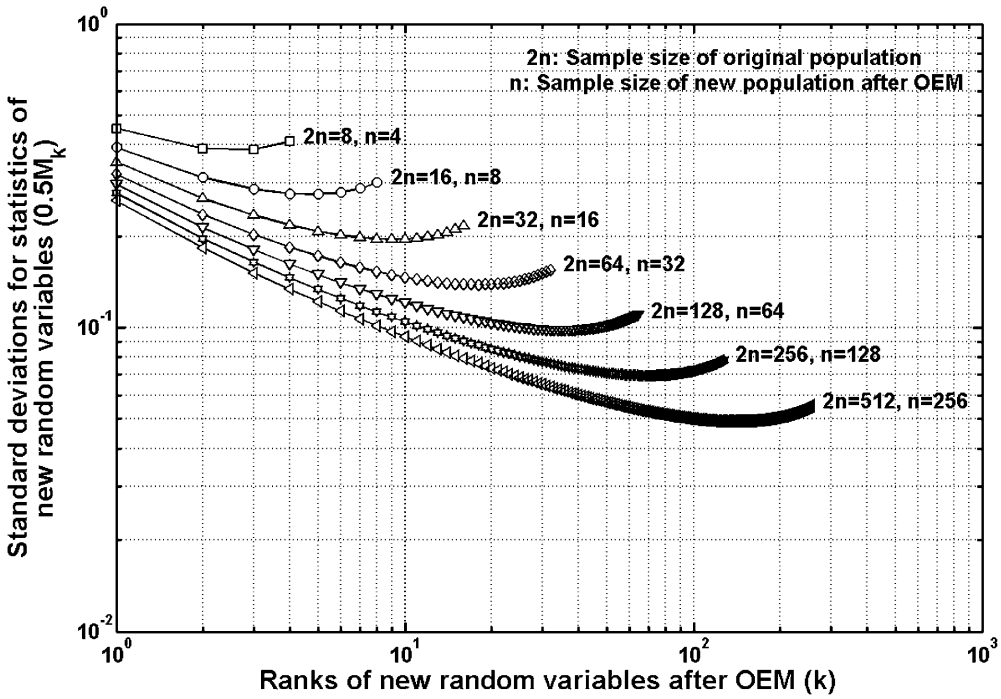

Figure 2.2 Standard deviations for statistics of new random variables after OEM ($0.5M_k$) in different sample population cases

Table 2.1 Average variation reduction after OEM in different sample population cases

Population size original (2n)	Population size after OEM (n)	Average standard deviation reduction
8	4	2.45
16	8	3.36
32	16	4.68
64	32	6.56
128	64	9.24
256	128	13.04
512	256	18.42

2.3 Outlier elimination

The standard deviation reduction factors by applying the OEM theory are considerably degraded due to the low rank samples in the new population M_k. These

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samples are equivalent in representing the lower and upper tails of the ordered sample population. In other words, the OEM theory is very sensitive to the outlying values of the original sample population. To further boost the error compensation efficiency, we propose a systematic strategy to eliminate a certain number of those samples. The details of the outlier elimination strategy are explained in the following subsections.

2.3.1 Outlier definition

As shown in Figure 2.2, for a fixed sample population size the standard deviation of $0.5M_k$ starts out at a large value, and drops quickly to a minimum, and then recovers slightly as continuously increasing the k value. Followed by this trend, we can use the last standard deviation value in M_k, i.e., σ_n, as a reference to set the threshold for the outliers in M_k. Hence, the outliers are defined as a sample collection from M_k that satisfies the following condition:

$$\sigma_k > g \cdot \sigma_n,\ 1 \le g \le \frac{\sigma_1}{\sigma_n}, \tag{2.28}$$

where g is a control factor that determines the number of outliers. When $g=\sigma_1/\sigma_n$, there is no outliers, because σ_1 is the maximum standard deviation; when g=1, all samples that have standard deviations greater than σ_n are removed from the sample population. A new variable q is introduced as the number of outliers in the population M_k. The lower limit for q is 0, whereas the upper limit is determined by the case when g=1.

Therefore, the outliers in M_k will always fall into the low rank categories. Suppose we have outliers with sample size of q in M_k, they are simply the first q samples, i.e., $M_1, M_2 \ldots M_q$. Recall (2.13), then the corresponding outliers in the ordered

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sample population $Z_{(i;2n)}$ are $(Z_{(1;2n)}, Z_{(2n;2n)})$, $(Z_{(2;2n)}, Z_{(2n-1;2n)})$ … $(Z_{(q;2n)}, Z_{(2n-q+1;2n)})$, which represent the lower and upper tails of the original sample population.

2.3.2 Outlier elimination strategy

The outlier elimination strategy is to symmetrically chop off q samples at each end of the ordered population $Z_{(i;2n)}$. In order to integrate the outlier elimination into the OEM procedure, we first still sort out the original component population according to their parameter orders. The next step is to omit q outliers at both tails of the ordered population. Followed by that, the pairing and summing steps take place.

By cutting the outliers in the ordered sample population, we are able to create a new component population with much smaller variations. Here, the symmetrically truncated population can be expressed as $Z_{(q+1;2n)} \le Z_{(q+2;2n)} \le \ldots \le Z_{(2n-q;2n)}$, and the new population after the pairing and summing steps can be rewritten as M_{q+1}, M_{q+2} … M_n, where

$$M_p = Z_{(p;2n)} + Z_{(2n-p+1;2n)},\ q+1 \le p \le n. \tag{2.29}$$

2.3.3 Standard deviation reduction enhancement

As mentioned above, the maximum value for q is determined by (2.28) when g=1. This case is referred as the maximum outlier elimination and will be used in the illustration of variation reduction enhancement. In order to provide reasonable comparisons, we shall keep the population size after the outlier elimination and OEM procedures as 4, 8, 16, 32, 64, 128 and 256. Then, 2q samples are intentionally added in

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the original population Z to accommodate the sample truncation. The value of 2q is determined by repeating the maximum outlier elimination process in differently sized sample populations until the resulting population size matches the desired value. Followed by this procedure, the original population sizes 2n are taken to be 10, 20, 40, 82, 164, 326, and 652, whereas the corresponding outlier numbers 2q are 2, 4, 8, 18, 36, 70, and 140. It is interesting to notice the percentage of outlier numbers, i.e., 2q/2n=q/n, is about the same for all population cases which is 21% on average. This observation actually gives the upper limit of q as 0.21n.

The variation reduction factors can be derived by using the same strategy as discussed in the previous section. The standard deviations have to be compared between random variables Z_i and $0.5M_p$. Intuitively, the standard deviations of $0.5M_p$ should be equal to the standard deviations of the remaining random variables in $0.5M_k$ where the first q samples are trimmed off. However, the true standard deviations are slightly different since the statistical characteristics of the original population have been modified by the sample truncations. We will come back to this problem in the following subsection. For the present stage, we consider the impacts of the sample truncations on the standard deviations by introducing a normalization factor f, where

$$f = \frac{2n-2p}{2n} = \frac{n-p}{n}. \tag{2.30}$$

The true standard deviations, denoted as σ_p^*, can be expressed by multiplying f to the standard deviations of the remaining random variables in $0.5M_k$, i.e.,

$$\sigma_p^* = f \cdot 0.5\sigma_k,\ q+1 \le k \le n. \tag{2.31}$$

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The resulting standard deviations for different sample population sizes are calculated and compared in Figure 2.3. It is clear that the standard deviations in each case are very close to uniformity after applying the maximum outlier elimination.

Now, we can calculate the new variation reduction factors B_p by taking the ratio of standard deviations of Z_i to the true standard deviations of $0.5M_p$:

$$B_p = \frac{1}{\sigma_p *}. \tag{2.32}$$

The average reduction factors for different sample populations are concluded in Table 2.2. Comparing to Table 2.1, the variation reduction is enhanced by a factor of 1.5. From this observation only, the variation reduction enhancement by applying the outlier elimination strategy may not be so promising; however it shows dramatic improvements on the DNL performance which will be demonstrated later.

The continuous variation reductions are accompanied by the cost of additional samples. By taking the ratio of the additional sample size to the original sample size as given in Table 2.1, a 27% overhead is required for maximum outlier elimination. However, maximum outlier elimination is still optimal in the sense that (a) if fewer extreme components are thrown, the worst case mismatch after OEM is due to those extreme pairs and it is expected to be larger; and (b) if more are thrown, the worst case mismatch is expected to be from pairs near "n". Practically, one should choose the outlier number q by considering a trade-off between design effort and optimally utilizing the outlier elimination strategy.

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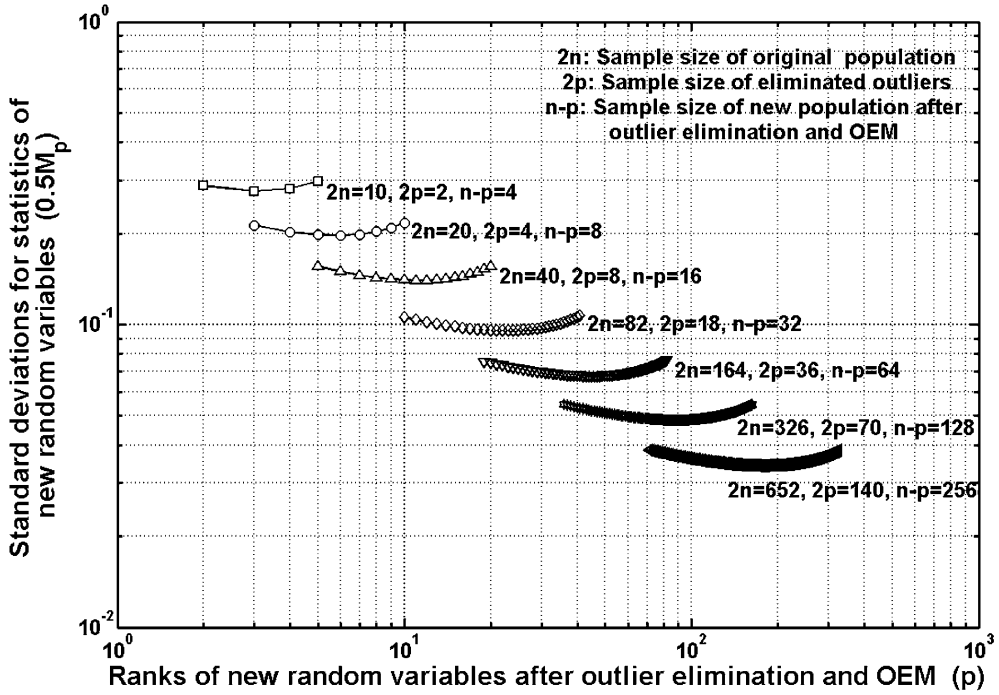

Figure 2.3 Standard deviations for statistics of new random variables after maximum outlier elimination and OEM ($0.5M_p$) in different sample population cases

Table 2.2 Average variation reduction after maximum outlier elimination and OEM in different sample population cases

Population size original (2n)	Population size after outlier (2n-2q)	Population size after OEM (n-q)	Average standard deviation reduction
10	8	4	3.51
20	16	8	4.89
40	32	16	6.87
82	64	32	10.08
164	128	64	14.24
326	256	128	19.93
652	512	256	28.18

2.3.4 Statistical analysis for outlier elimination

The standard deviation reduction by outlier elimination is simply due to the symmetrical truncation in the ordered population $Z_{(i;2n)}$. The amount of truncations can

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be defined as α at the lower tail and 1-β at the upper tail, where

$$\alpha = \frac{q}{2n}, \tag{2.33}$$

$$1-\beta = \frac{q}{2n}, \tag{2.34}$$

$$0 < \alpha < \beta < 1. \tag{2.35}$$

The sample population after outlier elimination, i.e., $Z_{(q+1;2n)} \leq Z_{(q+2;2n)} \leq \ldots \leq Z_{(2n-q;2n)}$, can be treated as the order statistics of random variables V_1, V_2 … V_{2n-2q} from a doubly truncated standard Gaussian population V. It truncates the original population below a and above b, where

$$\Pr\{Z \leq a\} = \alpha, \tag{2.36}$$

$$\Pr\{Z \geq b\} = 1-\beta. \tag{2.37}$$

The values of a and b can be easily obtained based on (2.4),

$$a = F_Z^{-1}(\alpha), \tag{2.38}$$

$$b = F_Z^{-1}(\beta). \tag{2.39}$$

Because the standard Gaussian population is truncated in a symmetric fashion, a and b are related by

$$a = -b, \tag{2.40}$$

$$f_Z(a) = f_Z(b). \tag{2.41}$$

The PDF and CDF of the doubly truncated standard Gaussian population, i.e., $f_V(v)$ and $F_V(v)$, can be obtained from [40]:

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$$f_V(v) = \frac{1}{(\beta-\alpha)\sqrt{2\pi}} \exp\left(-\frac{v^2}{2}\right) = \frac{f_Z(v)}{\beta-\alpha},\ a \le v \le b, \tag{2.42}$$

$$F_V(v) = \int_a^v f_V(t)\,dt = \frac{F_Z(v) - F_Z(a)}{\beta-\alpha}. \tag{2.43}$$

The expected value μ' and variance σ'^2 are obtained by:

$$\mu' = \frac{f_Z(a) - f_Z(b)}{\beta-\alpha}, \tag{2.44}$$

$$\sigma'^2 = 1 + \frac{a \cdot f_Z(a) - b \cdot f_Z(b)}{\beta-\alpha} - \left(\frac{f_Z(a) - f_Z(b)}{\beta-\alpha}\right)^2. \tag{2.45}$$

Based on (2.40) and (2.41), we can simplify (2.44) and (2.45) as:

$$\mu' = 0, \tag{2.46}$$

$$\sigma'^2 = 1 + \frac{2a \cdot f_Z(a)}{\beta-\alpha}. \tag{2.47}$$

The standard deviation enhancement factor C is just the standard deviation ratio between the original and truncated sample populations, which can be written as:

$$C = \frac{1}{\sigma'}. \tag{2.48}$$

To verify (2.48), we consider the case of maximum outlier elimination. The outlier number q is approximately equal to 0.21n as mentioned previously. By substituting this relation in (2.33) and (2.34), we can calculate α and β to be 0.105 and 0.895, respectively. The corresponding a and b values are -1.2536 and 1.2536. The

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obtained new standard deviation for the truncated population is about 0.65, and the enhancement factor is around 1.54, which matches our comparison between Table 2.1 and 2.2.

2.4 Complete-folding technique

We have theoretically demonstrated the OEM theory is very effective to reduce the standard deviations of random mismatch errors in a matching-critical component population. Based on this theory, a new random mismatch compensation technique, called complete-folding, is developed. It generates a well matched binary-weighted array from a unary-weighted array according to the component parameter orders.

2.4.1 Single-folding operation

To understand the functionality of complete-folding technique, we have to first consider single-folding operation. Here, a current source array is taken as an example. Single-folding operation is directly based on the OEM theory, in which a similar sequence of sorting, pairing and summing procedure is performed. The only difference is that an odd number of original samples are adopted, rather than the even number used in the previous derivation.

Figure 2.4(a) illustrates the three steps of single-folding operation for a 3-bit unary-weighted array that has 7 current sources in total. The rectangle in the figure denotes for the current value of each current source with random mismatch error. At the beginning, all current sources are sorted in the ascending order according to their

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magnitudes. Then, the complementary ordered current sources are paired, and the current source in the middle is left alone. Finally, two current sources in each pair are summed together, and the single current source is moved to the end of the new array. By doing so, we have generated a new unary-weighted current source array with sample size of 3, and their current values are approximately twice as large as the last single current source. More importantly, the random variations in current values are reduced significantly.

The new current source array actually represents a segmentation of 2-bit unary-weighted and 1-bit binary-weighted. In general, by applying the single-folding operation, an N-bit unary-weighted array can be converted into a segmentation of (N-1)-bit unary-weighted and 1-bit binary-weighted.

2.4.2 Complete-folding operation

If single-folding operation is continuously applied to the new unary-weighted array, eventually the N-bit unary-weighted array becomes an N-bit binary-weighted array. The entire folding process is therefore named as complete-folding. In other words, complete-folding is to implement (N-1)-time single-folding in an N-bit unary-weighted array. In the previous example of a 3-bit current source array, only 2-time single-folding is required to accomplish the complete-folding process. Figure 2.4(b) shows the second single-folding operation. It is noted only three current sources are left at the end, and they are differed by a factor of 2. Furthermore, the parameter variations are continuously diminishing compared to the results in the first single-folding operation.

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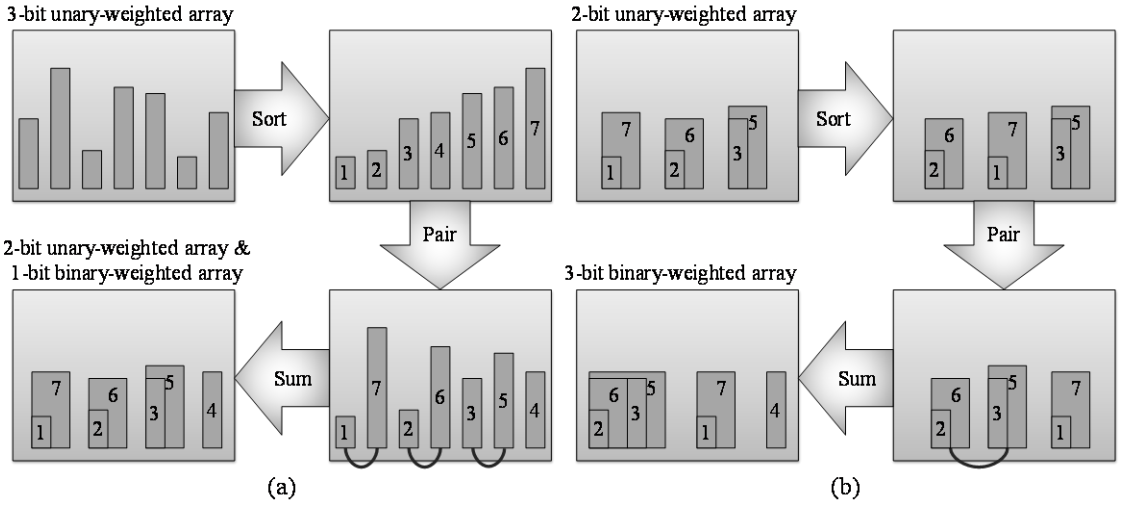

Figure 2.4 (a) 1st single-folding and (b) 2nd single-folding for a 3-bit unary-weighted current source array

2.4.3 Matching performance improvement

The resulting variation reductions by complete-folding technique can be understood with the help of the OEM theory. In the single-folding operation, the remaining single component represents the median of the N-bit unary-weighted array, where its expected value is the same as the expected value of the entire population. This feature is clearly addressed by our previous statistical analysis. The N-bit unary-weighted array contains 2n-1 elements, where $n=2^{N-1}$. The normalized error population Z has the same amount of random variables and follows standard Gaussian distribution. After the sorting process, the median of the population can be expressed as $Z_{(n;2n-1)}$. From the moment identities given in [40], the expected value of $Z_{(n;2n-1)}$ is:

$$\mu_{(n;2n-1)} = 0. \tag{2.49}$$

Hence, the middle ranked component statistically possesses the least error to the design value of all components. On the other hand, all other summed components also

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show much smaller parameter variations because of the OEM operation. As a result, the new segmented array exhibits superior matching accuracy compared to that of the original unary-weighted array. Followed by this, each single-folding operation brings some variation reduction, because the produced new sample population can be approximated by a Gaussian distribution [42]. However, it should be pointed out the most matching improvements are given by the very first number of single-folding operations within the complete-folding mechanism. This is not surprising because, as the folding process continues, the sample size under the treatment keeps shrinking and the resulting improvement factor becomes rather small, as shown in Table 2.1.

2.4.4 Outlier elimination integration

In order to further improve the matching accuracy, the outlier elimination strategy is integrated into the complete-folding technique. In practice, a certain number of additional components are introduced into the original component array, and then those largely defected components are omitted during the first single-folding operation. The corresponding outlier numbers for maximum outlier elimination can be determined from Table 2.2.

For a better conceptual illustration, a 7-bit unary-weighted component array is set as an example. This array originally contains 127 components. After adding 36 extras, the sample size becomes 163. Based on the outlier elimination strategy, the first and last 18 ordered components are omitted to ensure the obtained new sample size is the same as the original one. Once this process is finished, the complete-folding process is

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performed. It is noticed a significant enhancement in the variation reduction can be achieved for the first single-folding operation as shown in Table 2.2.

2.4.5 Implementation

To implement the complete-folding technique, two important functions have to be realized. One is to obtain the ranks of component parameters, and the other one is to make the routing to each component fully addressable. A simple block diagram for a potential circuit realization is given in Figure 2.5. In this approach, every two components in the N-bit unary-weighted array are compared by either voltage or current through a comparator. The output is used in a digital processing block for component sorting and pairing operations. Then, each component is assigned to an appropriate address via a register bank. The same address code obtained by different components indicates the fact that they have been summed together for the purpose of reducing random variations.

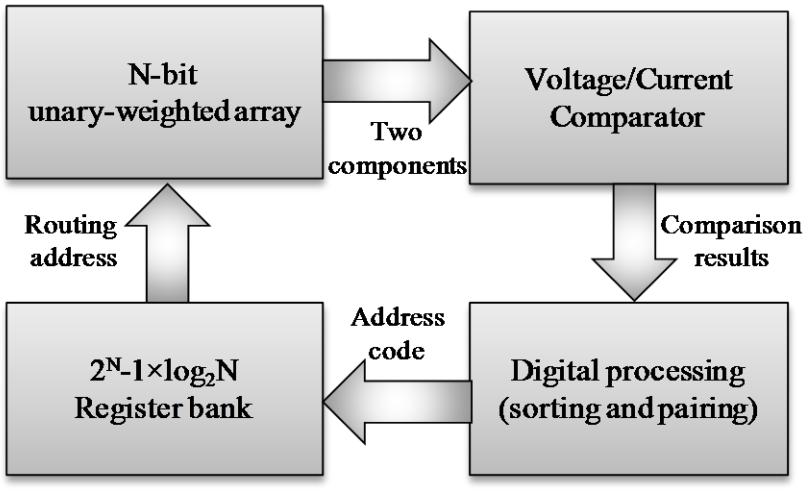

Figure 2.5 Block diagram of a circuit realization for complete-folding technique

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The digital processing block can be easily implemented if an efficient sorting algorithm is applied. Meanwhile, thanks to the binary-weighted operation, there are only N possible routing addresses for the N-bit component array. Therefore, the width of the register bank is only $\log_2 N$ bits. On the other hand, the depth of the register bank is determined by the total number of components, i.e., 2^N-1.

When the complete-folding is applied to a reasonably sized component array with presented system blocks, the digital complexity can be easily managed. Nevertheless, this circuit realization might not be the best choice in every data converter design. A better implementation could be found once one has a thorough understanding of the specific circuits where complete-folding is utilized.

2.5 Statistical simulation results

A number of statistical simulations are carried out to test the efficiency of the complete-folding technique that is cooperated with the OEM theory. In this work, an N-bit unary-weighted current source array is used to conduct the simulations, where N may vary in the different simulation cases. This component array can be treated as the building block of the most significant bits (MSBs) in a 14-bit data converter design. It is well known that the static performance of a data converter strongly depends on the linearity of MSBs. Therefore, the matching performance of this component array plays a key role in determining the ultimate performance potential and design cost of the data converter. In the following discussions, the unit of LSB (least significant bit) always refers to the LSB at the 14-bit level.

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It is also important to know random mismatch is the only considered source of error in these simulations. Other sources of errors in a current source array such as gradient errors and errors due to finite output impedance are assumed to be managed by the existing design techniques. To compensate gradient errors, each current source can be divided into 4 or more subunits so that special layout strategies can be applied. To compensate errors due to finite output impedance, one can use cascode transistors, or if voltage headroom is a concern, one can implement the design technique presented in [43].

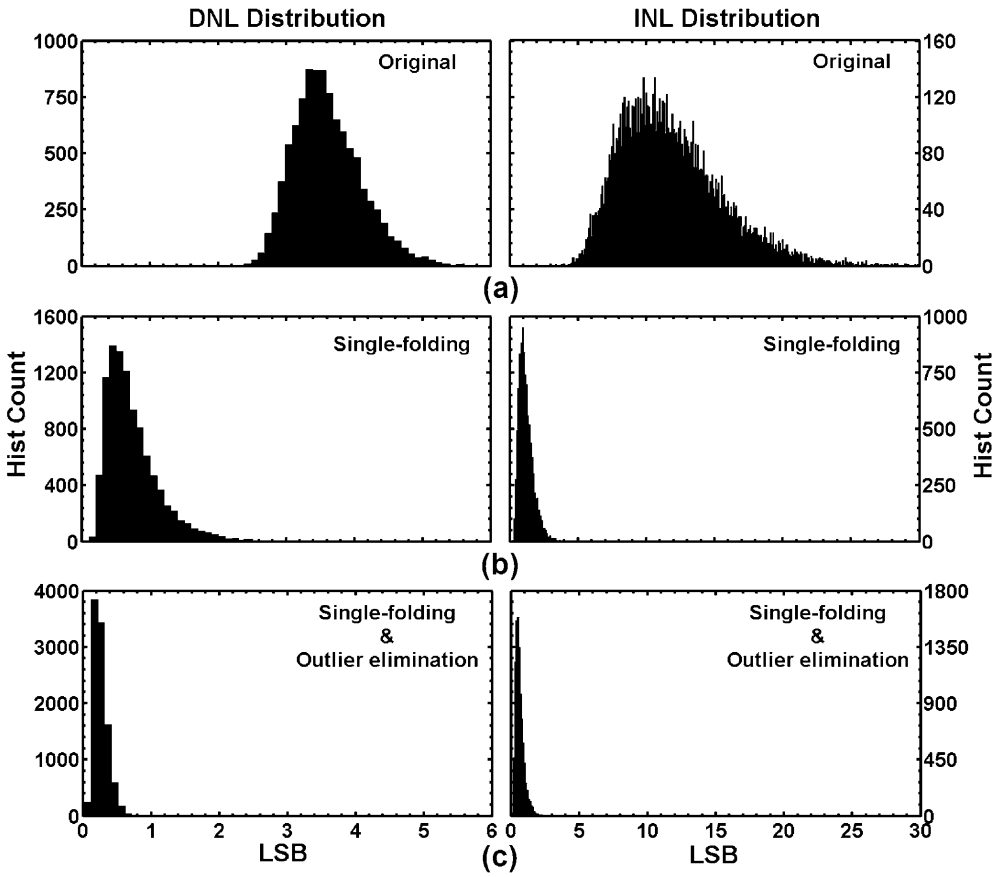

Figure 2.6 DNL and INL distributions for 10,000 randomly generated 7-bit MSB arrays in a 14-bit data converter design with σ_{MSB}=1%: (a) original, (b) after single-folding, (c) after maximum outlier elimination and single-folding

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Table 2.3 DNL and INL improvements after single-folding in different MSB arrays

Number of bits of MSB array (N)	DNL improvement	INL improvement
3	2.29	3.26
4	2.83	4.08
5	3.39	5.40
6	4.11	7.20
7	4.81	9.82
8	5.50	13.25
9	6.39	18.04

Table 2.4 DNL and INL improvements after maximum outlier elimination and single-folding in different MSB arrays

Number of bits of MSB array (N)	Outlier number (2q)	DNL improvement	INL improvement
3	2	3.47	4.55
4	4	4.70	6.17
5	8	6.58	8.77
6	18	9.92	13.03
7	36	14.03	18.18
8	70	20.37	25.92
9	140	29.90	36.74

2.5.1 Single-folding without outlier elimination

In this subsection, the linearity improvements by applying single-folding to the N-bit MSB array are investigated, where N is taken as 3, 4, 5, 6, 7, 8, and 9. For each N, 10,000 MSB arrays are randomly generated based on a relative standard deviation of the unit current source (σ_{MSB}). This standard deviation can be arbitrarily chosen (e.g., 1%), because our primary goal is to examine the linearity improvement factors, which are defined as the average ratio of the DNL and INL before and after applying single-folding.

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Figure 2.6(a) and (b) present the DNL and INL distributions for 10,000 randomly generated 7-bit MSB arrays in a 14-bit data converter design before and after single-folding operations with σ_{MSB}=1%. Clearly, both DNL and INL distributions become narrower. It is also worth mentioning the 7-bit unary-weighted MSB array is now transformed into a segmentation of 6-bit unary-weighted and 1-bit binary-weighted. For other N values, the DNL and INL distributions follow the same trends as the N = 7 case. Table 2.3 summarizes the DNL and INL improvement factors for all simulated cases.

From the theoretical perspective, the single-folding is straightly based on the OEM theory. Therefore, the DNL improvement factors shown in Table 2.3 are expected to represent the standard deviation improvement factors given in Table 2.1. However, they are actually quite different from each other. This is because the DNL after single-folding operation is dominated by the outlying summed components in the new segmented array. As shown in Figure 2.2, those components have much larger standard deviations than the others, and as a result their improvement factors will be much less than the average factors shown in Table 2.1. Meanwhile, the INL performance after single-folding also becomes appealing because of the fact that it is associated with the DNL improvements.

2.5.2 Single-folding with maximum outlier elimination

So as to enhance the linearity performance, maximum outlier elimination strategy is integrated into the single-folding operation, where extra components are added to the original component array. The number of extra components added in each case is

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obtained from Table 2.2, i.e., 2, 4, 8, 18, 36, 70 and 140. All other simulation setups are kept the same as the previous subsection.

Figure 2.6(c) shows the new DNL and INL distributions for 10,000 randomly generated 7-bit MSB arrays after integrating maximum outlier elimination strategy. A considerable amount of improvements in both linearity distributions is observed compared to Figure 2.6(b). Table 2.4 concludes the DNL and INL improvement factors in different simulations. It is illustrated that the DNL and INL improvement factors are significantly enhanced by integrating the maximum outlier elimination strategy. For MSB arrays whose resolutions are greater than 5, the DNL performance is enhanced at least by a factor of 2.

Meanwhile, it is also interesting to notice the DNL improvement factors perfectly match the calculated standard deviation improvement factors as given in Table 2.2. This is anticipated because the maximum outlier elimination strategy has made all the components close to uniformity after the single-folding operation, and their standard deviations are almost the same as shown in Figure 2.3. Therefore, the DNL improvements are directly related to the average standard deviation improvements.

2.5.3 Complete-folding with maximum outlier elimination

By embedding the maximum outlier elimination strategy into the complete-folding technique, it is able to further increase the linearity performance of the MSB array. We shall illustrate this point by performing a statistical simulation, where N is set to be 7. Followed by the general process for complete-folding, we employ the 6-time

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single-folding to the 7-bit MSB array. In addition, 36 extra current sources are added, but only 127 current sources are used when the maximum outlier elimination process is completed

For the purpose of studying the linearity improvements by complete-folding, we intentionally break up the entire process into 6 steps. Figure 2.7 shows the DNL and INL distributions of 10,000 randomly generated 7-bit MSB arrays after each single-folding with σ_{MSB}=1%. Table 2.5 summarizes the linearity improvement factors after each single-folding operation compared to the original static accuracy.

Noticeably, each single-folding improves the overall DNL and INL; however, the improvement factors become less significant after each single-folding. The greatest improvement factors are attributed by the first three single-folding operations. Comparing to the linearity performance by single-folding and outlier elimination, complete-folding and outlier elimination improves DNL and INL by another factor of 3 and 9, respectively. All of these observations justify our previous statistical analysis.

Table 2.5 DNL and INL improvements after each single-folding in a 7-bit unary-weighted MSB array

Step	DNL improvement	INL improvement
Original	1	1
1st single-folding with outlier elimination	14.00	18.30
2nd single-folding	28.27	60.87
3rd single-folding	35.04	107.72
4th single-folding	38.31	140.22
5th single-folding	39.86	153.68
6th single-folding	40.43	157.20

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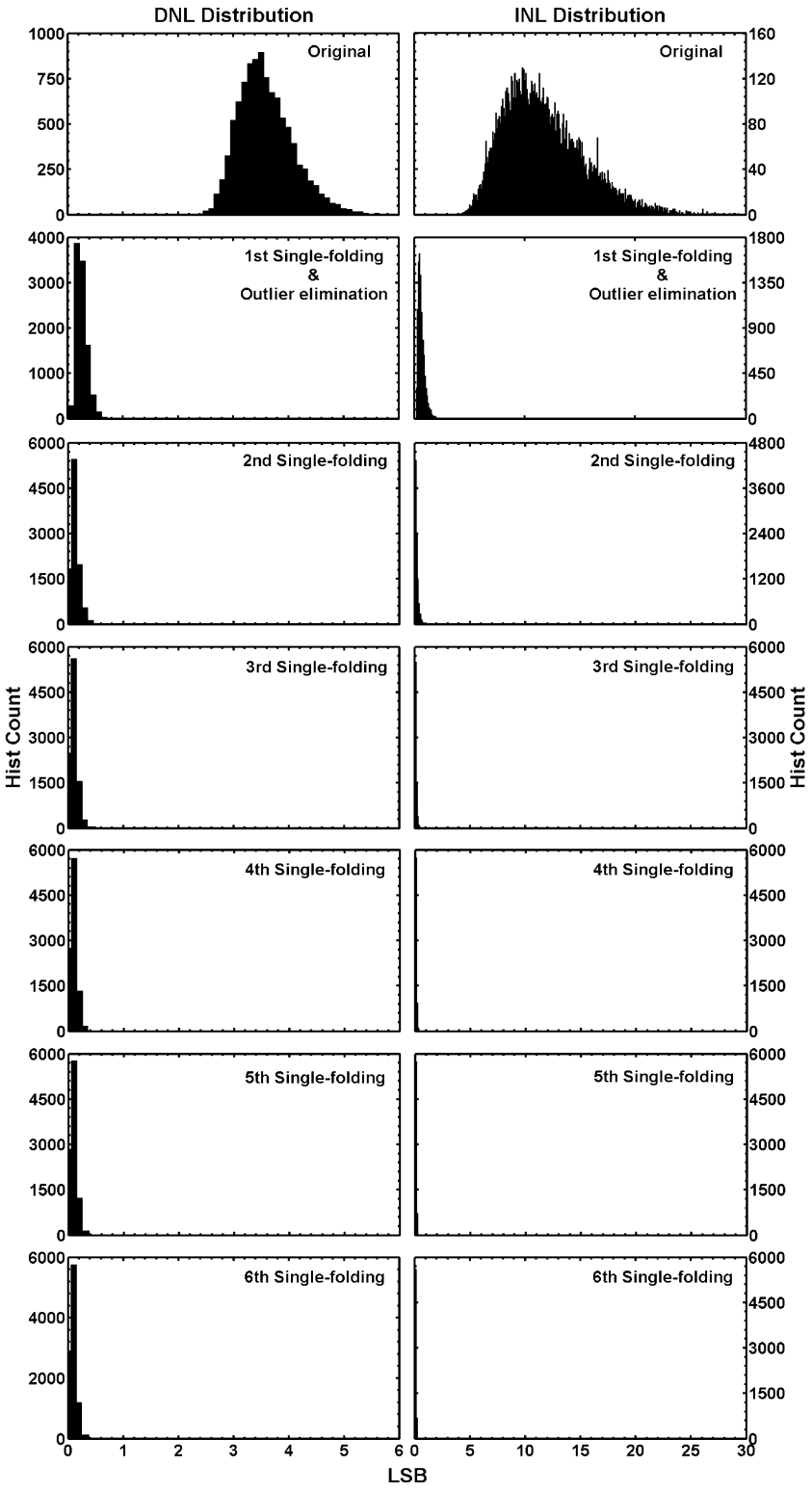

Figure 2.7 DNL and INL distributions of 10,000 randomly generated 7-bit MSB arrays in 14-bit data converter design after each single-folding with σ_{MSB}=1%

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2.5.4 Matching performance comparisons with state of the art

Complete-folding with maximum outlier elimination has shown promising potential for compensating random mismatch errors in the matching-critical components. Here, we will compare our technique with the other two leading techniques in the literature. The first technique being considered is called self-calibration [17]. It uses an accurate calibration ADC (CALADC) to digitally characterize the data converter's output errors and feeds back analog correction signals to the output by a calibration DAC (CALDAC). The second technique is called switching sequence post adjustment (SSPA) [18]. It places a component having small error in neighbor with the one having large error. Outlier elimination is also used in this technique for better matching performance.

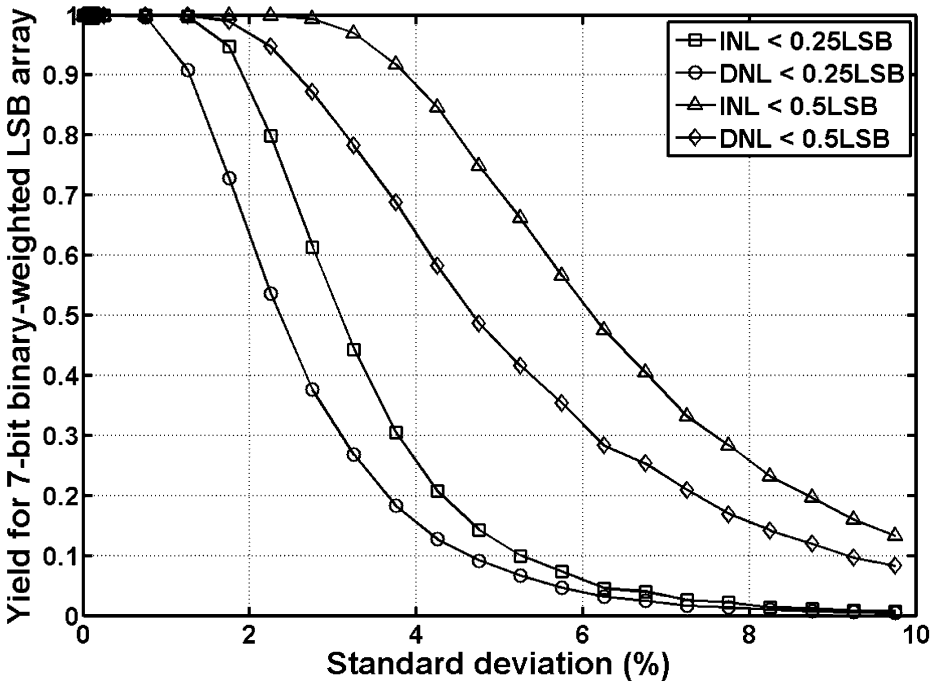

Figure 2.8 Yield estimation for the 7-bit LSB binary-weighted array with different linearity conditions

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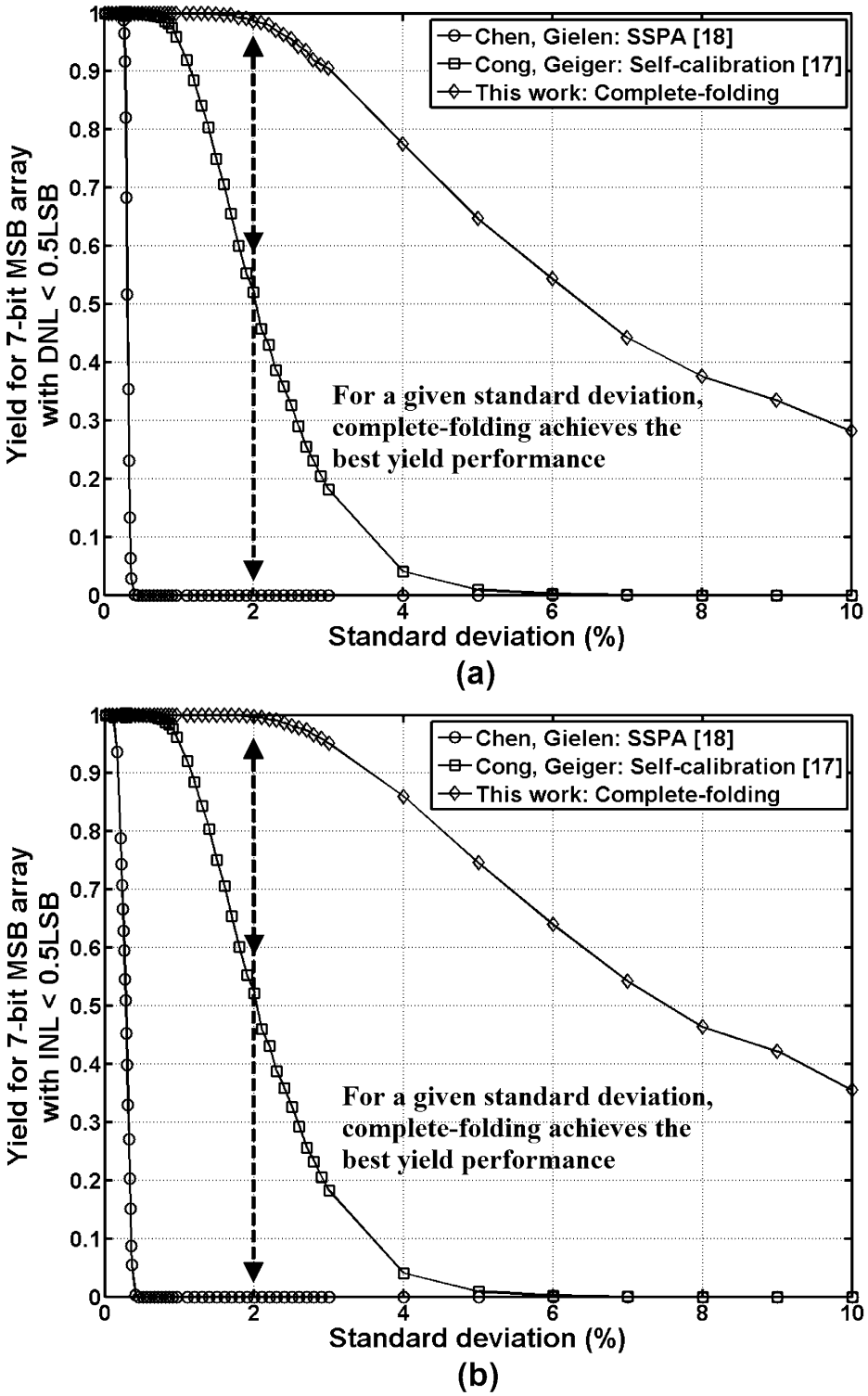

Figure 2.9 Yield estimations for the 7-bit MSB unary-weighted array with (a) DNL < 0.5LSB and (b) INL < 0.5LSB by separately applying self-calibration, SSPA and complete-folding techniques

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In the following discussion, each technique mentioned above is implemented into the MSB array and the corresponding area reduction for the 14-bit data converter is derived from Monte Carlo simulations. More specifically, we will consider a 14-bit current-steering DAC as an example, which possesses 7-7 segmentation, i.e., 7-bit unary-weighted MSB array and 7-bit binary-weighted LSB array. The desired yield of this 14-bit DAC is set to be 99.7% with DNL < 1LSB and INL < 1LSB. In order to achieve such matching performance without employing any techniques, the standard deviation of a unit LSB current source has to be at most 0.42%.

In our simulations, we conservatively assume both MSB and LSB arrays contribute to a half of the total error budget (0.5LSB) and they are uncorrelated. We use a sufficiently large circuit area for the LSB array to achieve the desired matching accuracy. Figure 2.8 presents the yield estimations by Monte Carlo simulations for the 7-bit LSB array under different linearity conditions. In order to achieve 99.7% yield with DNL < 0.5LSB and INL < 0.5LSB, the standard deviation of the unit LSB current source has to be at most 1.5%.

Table 2.6 Maximum standard deviations of unit current source to achieve 99.7% yield with different linearity conditions in a 7-bit MSB unary-weighted array by different techniques

Technique	σ_{MSB} DNL <0.5LSB	σ_{MSB} INL <0.5LSB
Chen, Gielen: SSPA [18]	0.25%	0.11%
Cong, Geiger: Self-calibration [17]	0.7%	0.7%
This work: Complete-folding	1.6%	1.9%

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Table 2.7 Current source area comparison by different techniques for a 14-bit current-steering DAC

Technique	MSB Area	LSB Area	Total Area	Area Reduction
Large area	$16256S_u$	$127S_u$	$16383S_u$	1
Chen, Gielen: SSPA [18]	$2376.3S_u$ [a]	$10.0S_u$	$2386.3S_u$	6.9
Cong, Geiger: Self-calibration [17]	$45.7S_u$	$10.0S_u$	$55.7S_u$	294.1
This work: Complete-folding	$11.2S_u$ [a]	$10.0S_u$	$21.2S_u$	772.8

[a]The area of additional current sources are included in the MSB area calculation.

On the other hand, we apply different techniques to the 7-bit MSB array. Monte Carlo simulations are performed for each case. Before jumping into the simulation results, it is worth mentioning the different setup for each technique. In the self-calibration case, both errors from CALADC and CALDAC are limited to 0.25LSB, where CALADC is set to have 16-bit resolution and accuracy and CALDAC has 8-bit resolution [17]. Moreover, 36 extra current sources are added for both SSPA and complete-folding techniques. Again, only 127 current sources are used by the end of outlier elimination process.

Figure 2.9(a) and (b) illustrate the yield estimations for the 7-bit MSB array by applying the three different techniques with DNL < 0.5LSB and INL < 0.5LSB. It is shown that for a given standard deviation, complete-folding technique achieves the best yield compared to SSPA and self-calibration techniques. In particular, the achieved performance is orders of magnitudes better than that using SSPA technique. Based on those, we can obtain the corresponding standard deviations of the unit MSB current

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source for a yield of 99.7% within the desired linearity conditions. The results are concluded in Table 2.6. Again, complete-folding technique shows significant advantages compared to the other two techniques.

To be more instructive, we convert both standard deviations of LSB and MSB arrays for different techniques into the total area requirement for a 14-bit DAC. The calculated results are included in Table 2.7. S_u represents the area for the unit LSB current source when we employ large area to compensate random mismatch errors, and the corresponding total area serves as a reference to obtain area reduction factor for each technique. Evidently, the complete-folding technique achieves the largest area reduction factor, which is about 773!

In addition, complete-folding technique will have major advancements in the circuit realization. Compared to self-calibration technique, complete-folding shifts most of the implementation circuitry into the digital domain which makes it compatible with IC technology scaling. On the other hand, complete-folding exhibits much less digital complexity than SSPA technique because of the full binary-weighted operation, where the binary-to-thermometer decoding is completely eliminated.

Furthermore, complete-folding technique can also relax the area associated with the component interconnections in circuit layout. As we mentioned before, the systematic gradient errors are managed by sophisticated layout strategies where each component is divided into 4 or more subunits for proper placement and interconnection. In the cases of self-calibration and SSPA techniques, the analog area is reduced, which gives small gradient errors and thus leads to relaxed layout sophistication. In contrast,

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complete-folding technique further reduces the analog area which results even smaller gradient errors. Most importantly, this technique can be applied to non-Gaussian mismatch errors as mentioned in the statistical analysis. Therefore, both local random mismatch errors and the small residual gradient errors can be simultaneously handled and there is no need for special layout strategies.

Based upon above, complete-folding features simplicity and compactness of its circuit implementation and a significant analog circuit area reduction by using this technique can be anticipated in many high-resolution high-accuracy data converter designs.

2.6 Conclusion

In this chapter, we have theoretically shown that the OEM theory together with the outlier elimination strategy are very effective for compensating random mismatch errors presented in a circuit component population. A new matching technique complete-folding is developed, where it utilizes the OEM theory multiple times to convert a poorly matched unary-weighted component array to a very well matched binary-weighted array. For the same yield requirement in a 14-bit DAC design, complete-folding shows a spectacular area reduction compared to state of the art.

Many data converters are particularly susceptible to the component variability caused by random mismatch errors which often plays a key role in determining the ultimate performance potential and production cost. Multi-bit sigma-delta modulator ADC, SAR (successive approximation register) ADC, current-steering DAC, and

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resistor-string DAC are just a few examples where a very well matched circuit component array is required for the success of their data conversion tasks. By applying the OEM theory to these data converter designs, all the process dependent mismatch errors can be eliminated and as a result, the analog area requirement is greatly reduced.

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CHAPTER 3

A 15-BIT BINARY-WEIGHTED CURRENT-STEERING DAC WITH ORDERED ELEMENT MATCHING

3.1 Introduction

High-resolution and high-accuracy DACs can be widely found in various medical, instrumentation, and test and measurement applications. For these types of circuits, device matching is one of the most critical design parameters. As IC technology continues to evolve, the minimum feature size is quickly approaching nanometer scale. In these technology nodes and beyond, significant variability, due to process, supply voltage, temperature, and stress, imposes grand challenges to achieving accurate device matching. With the emerging materials and devices that may provide an alternative to CMOS, variability is no less.

Traditional matching techniques can compensate random mismatch errors to certain degrees, but they possess some disadvantages. For example, trimming [11], [19] suffers high cost in terms of test equipments and time; calibration [16], [17] requires complicated compensation circuitry; switching sequence adjustment [18], [44] offers no improvements to differential nonlinearity (DNL); and dynamic element matching (DEM) [15], [32] limits its most applications to sigma-delta data converters.

A totally different approach called ordered element matching (OEM) was developed and rigorously proven using order statistics in Chapter 2. It first sorts largely mismatched unit elements based on their parameter orders, and then pairs and combines

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the complementary ordered ones to reduce the random variations significantly. After repeating multiple OEM operations in a unary-weighted element array with the presence of large variability, a well-matched binary-weighted array can be generated. Additionally, an outlier elimination strategy can be incorporated by putting in additional elements to enhance the matching performance. The underlying idea for the "binarization" process is that, proper interconnections and combinations can provide an effective system level matching that is several orders of magnitude better than what the original element population can reach. It converts a deadly concern of large random variations into a useful resource for improving matching performance.

In this chapter, a 15-bit current-steering DAC is designed and fabricated in a standard 130nm CMOS technology to demonstrate the significant linearity improvements by OEM. The DAC has 7-8 segmentation, where OEM is continuously applied to the 7-bit unary-weighted MSB array. By doing so, a 7-bit binary-weighted MSB array is formed at the end. The 8-bit LSB array has a conventional binary-weighted structure, therefore yielding an overall 15-bit binary-weighted DAC. The chip's active area is less than 0.42mm^2, among which the 7-bit MSB array only consumes 0.021mm^2. Measurement results show that the DNL can be reduced from 9.85LSB to 0.34LSB, whereas the INL can be reduced from 17.41LSB to 0.77LSB.

This chapter is organized as follows. In Section 3.2, the OEM binarization and outlier elimination and the ensuing effective system level matching are conceptually illustrated. Section 3.3 shows the DAC architecture and the associated circuit

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implementations. Followed by those, measurement results are provided in Section 3.4. Finally, conclusions are drawn in Section 3.5.

3.2 Concept illustration

3.2.1 OEM theory

Random mismatch in CMOS devices is due to inherent variations in the semiconductor process. It is by far the largest source of error degrading the performance of high-resolution and high-accuracy DACs. Based on the standard mismatch model [28], for a MOSFET in saturation with an overdrive voltage V_{gs}-V_t, the relative variance of the drain current is given by:

$$\left(\frac{\sigma_I}{I}\right)^2 = \frac{A_\beta^2 + 4A_{Vt}^2 / \left(V_{gs} - V_t\right)^2}{2 \cdot W \cdot L}, \tag{3.1}$$

where A_β and A_{Vt} are the process mismatch parameters, and W ŀ L is the gate area. Similar formulas for capacitor and resistor mismatch errors also show the variance inversely proportional to the area [24]-[26]. This leads to the basis of the widely used rule of thumb: quadrupling area for every factor-of-two reduction in random mismatch errors.

Nevertheless, instead of changing the design variables in (3.1), we can reduce standard deviation of the mismatch errors by combining a pair of complementary ordered components in a population. This process is called OEM. From statistical analysis in Chapter 2, the standard deviation can be reduced by a factor of at least 6.5 for a sample population size greater than 64 with one-time OEM iteration.

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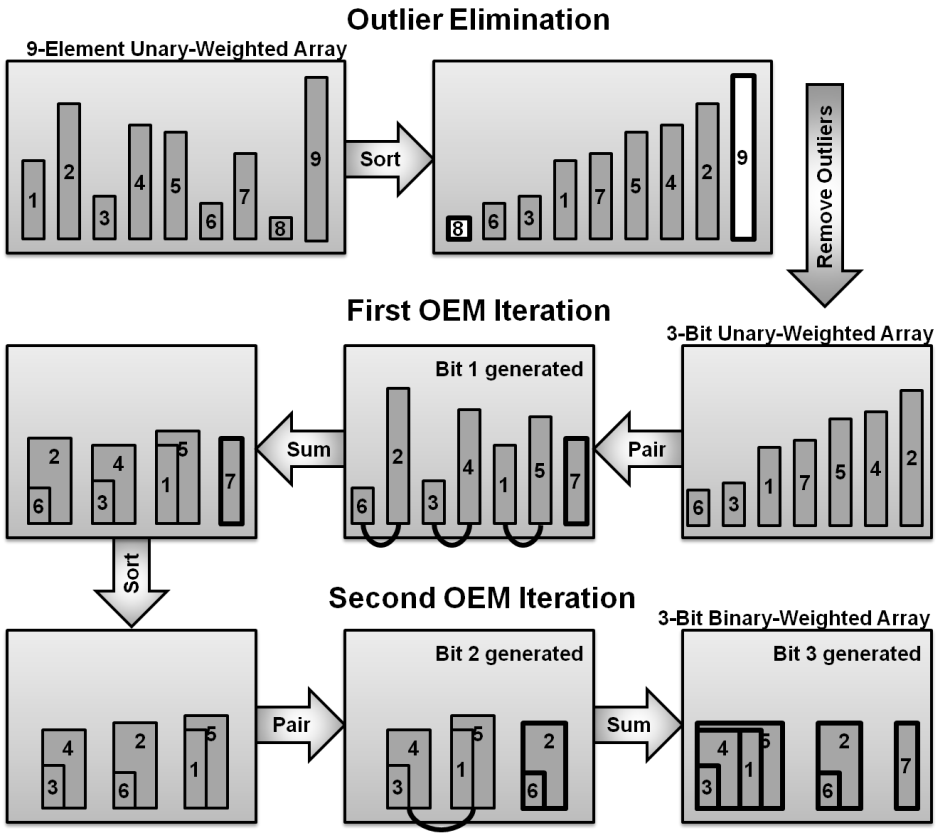

Figure 3.1 3-bit binary-weighted array generation based on outlier elimination and two OEM iterations from a 9-element unary-weighted array

3.2.2 OEM binarization and outlier elimination

To take advantage of the significant variance reduction offered by OEM, we can continuously apply the OEM operation in a mismatched unit element population, and then create a binary-weighted array that achieves an accurate system level matching. A 3-bit unary-weighted array is taken as an example for the whole process illustration. Since outlier elimination is proven to be effective in boosting the matching performance, we will start with 9 unary mismatched components. Figure 3.1 shows the outlier elimination step, which simply truncates the sorted element array by removing two

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outliers. The area of each rectangle in the figure denotes the value of each unit element with random mismatch error. Followed by outlier elimination, we can apply two OEM iterations to the remaining elements.

The specific steps proceed as follows. First, all elements are sorted in ascending order. Then, the complementary ordered elements are paired, and a single element in the middle is left alone. Finally, two elements in each pair are summed together, and the singleton is moved to the end of the array. Thus, we have generated a new 2-bit unary-weighted array with each element nearly twice the value of the original elements, and a 1-bit binary-weighted array. The random variations in the new elements are reduced significantly by the OEM theory. If we continue this process to the new unary-weighted array, only three elements are left at the end, and they differ by a factor of 2. Furthermore, the parameter variations are rapidly diminishing compared to the previous step. In general, n-1 OEM iterations are required to convert an n-bit unary-weighted array into an n-bit binary-weighted array.

3.2.3 Statistical characteristics of DNL and INL

The linearity performance advancements by the new matching techniques can be examined from the following study. In a mismatched unit element population, different element interconnections and combinations can yield different DNL and INL characteristics. The study in [45] considered two common cases, i.e., thermometer-coded and binary-weighted architectures. Here, we will incorporate OEM binarization and outlier elimination with the similar MATLAB simulations. First, 163 normally

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distributed unit elements are generated with a relative standard deviation of 1%. Then, by selecting 127 elements randomly, three different 7-bit structures such as conventional binary-weighted, thermometer-coded, and OEM based binary-weighted arrays, can be generated. Another 7-bit structure can be also considered in which OEM binarization and outlier elimination are used together to the 163 elements. Then, the DNL and INL can be obtained in the four different cases, and 10,000 simulations are repeated to find the standard deviations of DNL and INL from different code transitions. Figure 3.2 shows the corresponding simulation results.

Comparing the conventional binary-weighted array with the thermometer-coded array, we can draw the same conclusions as those in [45]. The INL standard deviations are about the same for both cases, where the maximum happens at the midscale with the value being about $0.5 \cdot \sqrt{128} \cdot 1\% = 5.7\%$. On the other hand, the DNL standard deviations are about 1% for all codes in the thermometer-coded array, whereas the maximum occurs at the midscale in the conventional binary-weighted array with its value equaling to $\sqrt{128} \cdot 1\% = 11.3\%$.

After applying OEM binarization, the linearity characteristics are improved considerably. The DNL standard deviation curve exhibits the similar behavior compared to the traditional binary-weighted array. The maximum at the midscale is about 0.33%, which is even less than the thermometer-coded case. Alternatively, the INL standard deviations also have the maximum coming about the midscale, and its value is around 0.17%. As incorporating outlier elimination, both metrics are continuously diminishing. The maximum DNL standard deviation is around 0.065% and still locates around the

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midscale. Furthermore, the DNL standard deviations at the other locations become comparable to the maximum. In contrast, the maximum INL standard deviation is 0.057%, and surprisingly, it takes place at the two tails instead of the midscale.

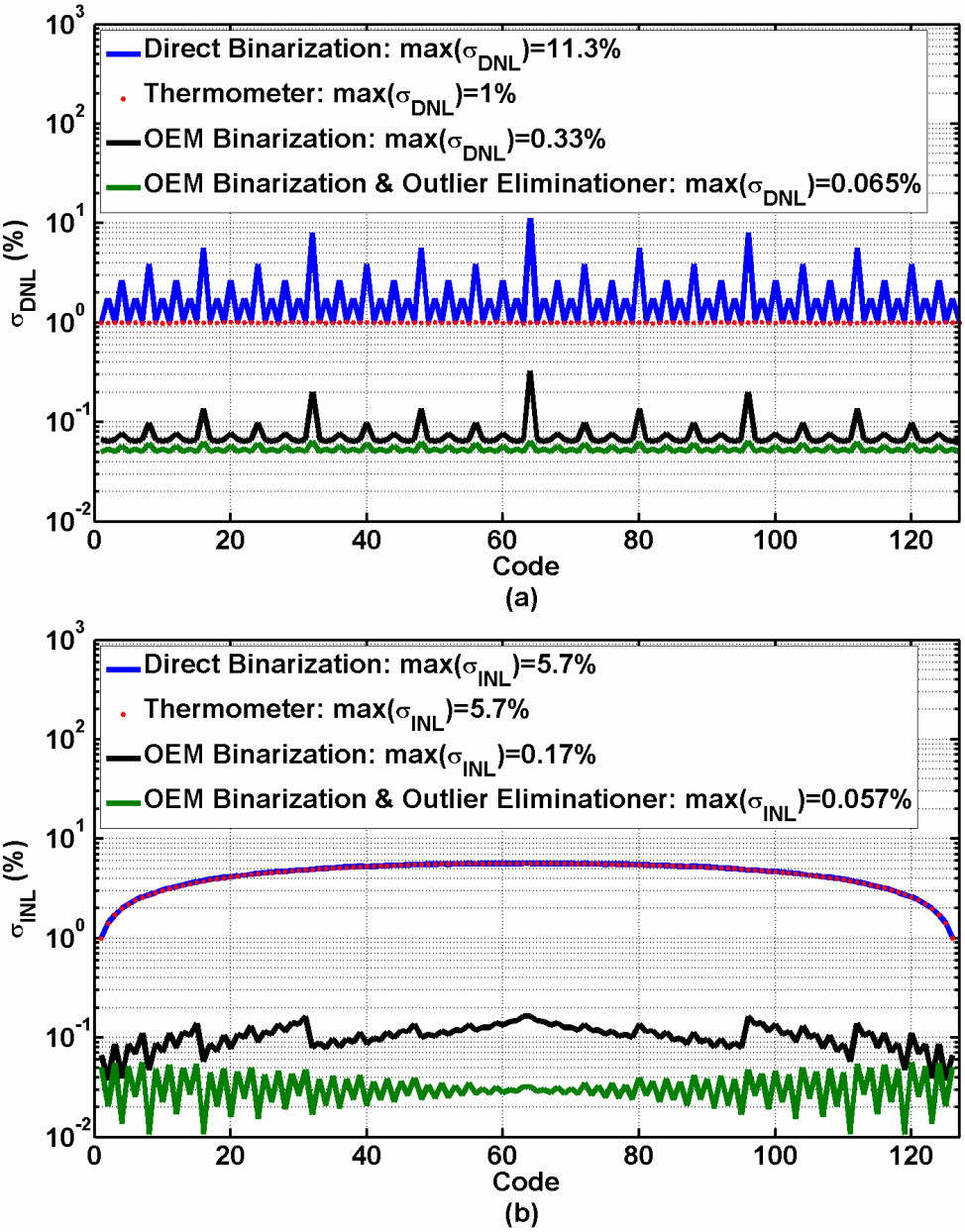

Figure 3.2 Standard deviations of (a) DNL and (b) INL in a 7-bit element array which is realized by direct binarization, thermometer decoding, OEM binarization, and mixture of OEM binarization and outlier elimination

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The obvious linearity improvements after OEM binarization and outlier elimination can be explained by the dramatic error variance reduction shown in Chapter 2. To obtain the exact theoretical formulas for the statistical characteristics of DNL and INL achieved by the new matching techniques, we have to deal with non-identical and non-independent order statistics in the analysis, which is extremely difficult. The key point for these simulations is to show that, proper interconnections and combinations in a population of devices with significant variability can create an effective system level matching that is significantly better than what the original devices can achieve. This enables us to continue pursuing accurate matching with the presence of large random variations in nanometer CMOS and emerging technologies.

3.2.4 Relative error standard deviations of resulting binary bits

From the above simulations, the maximum INL standard deviation moves from the midscale to the two tails while integrating outlier elimination into the OEM binarization. It is because that, the largest error standard deviation of the resulting binary bits is shifting from MSB to LSB. To illustrate this, we construct the following simulation by firstly generating a normally distributed unit element population with a relative standard deviation of 1% and sample size of $127\cdot(1+\delta)$, in which δ is the percentage of additional elements ($0\%\leq\delta\leq100\%$). Then, outlier elimination is applied to truncate the additional elements symmetrically if there are any. The OEM binarization takes place after subtracting the average from the remaining 127 elements for a meaningful conclusion. The upper limit of 100% is not a fundamental limit; however, it

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is chosen because that adding more than 100% elements will increase the effective array resolution number, and generating a higher resolution binary-weighted array by the new techniques will be more cost-efficient than the lower resolution case.

Figure 3.3 shows the relative error standard deviations of the 7 binary bits for δ varying from 0% to 100%. When δ=0%, it indicates that we only use OEM binarization. Indeed, the MSB has the largest error standard deviation. Once we include outlier elimination with 0%<δ≤100%, the relative error standard deviation associated with each bit reduces, and the curvature also changes where the maximum shifts from MSB to LSB. It should be also pointed out that the error standard deviations in all cases are much less than those of a typical binary-weighted structure.

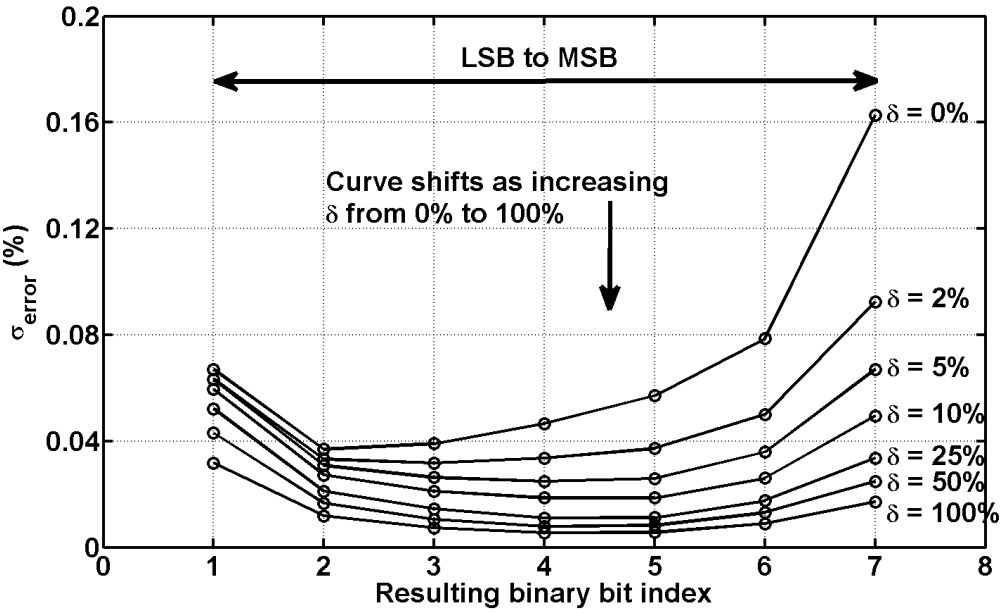

Figure 3.3 The relative error standard deviations of the resulting binary bits after applying OEM binarization with outlier ratio δ varying from 0% to 100%

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3.2.5 Optimal utilization of outlier elimination

As we can see, outlier elimination is highly beneficial to enhance the linearity performance. In Chapter 2, we thoroughly studied the case when δ=27%. This was referred as the maximum outlier elimination. The phrase is somewhat a misnomer. It is not about achieving the maximum linearity performance, but rather stands for the maximum number of outliers that can be thrown away without causing the outer pairs to have smaller error standard deviations than the middle pairs after a single OEM iteration, which is an arbitrary threshold.

For the optimal use of outlier elimination, we will consider the following simulation. A fixed analog area is pre-given, and we divide it into $(2^n-1)\cdot(1+\delta)$ elements. The variable n represents the number of bits for the desired element structure, and it varies from 3 to 9. At each n value, δ will change from 0% to 100%. For each combination of n and δ, we will use OEM binarization and outlier elimination in the corresponding element array to obtain the maximum DNL and INL, and then normalize them to those linearity quantities from a conventional binary-weighted structure under the same resolution and area constraints. It is worth mentioning that the area of the unit element may vary in different cases since the entire analog area is a fixed number. Alternatively, we can think that the outlier elimination is cost-free in terms of the analog area from this setup.

Figure 3.4 gives both of the normalized maximum DNL and INL corresponding to different cases. It is easy to see that outlier elimination becomes much more effective for the element array whose resolution is greater than 4. Furthermore, the most efficient

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linearity improvement comes at δ=10% in a single case. After this point, there are still improvements, but more outliers need to be added, and the associated design overhead may exceed the actual analog area reduction, e.g., digital circuitry area.

The nonlinearity reductions before δ=27% can be understood since we have eliminated the elements that contain large error standard deviations. Then, we should not have any improvements as increasing δ more. From Figure 3.4, this is certainly not the case. The slight linearity improvements afterwards can be explained as follows.

Outlier elimination will cause the LSB possess the largest error standard deviation as seen in Figure 3.3. Then, the most nonlinearity comes from this lowest bit that essentially represents the median element of the original population. The asymptotic standard deviation of the median in a sample population can be written [40] by:

$$\sigma_{\text{median}} = \sqrt{\frac{\pi}{2N}} \cdot \sigma_{\text{unit}}, \tag{3.2}$$

where N is the total number of elements, and σ_{unit} is the standard deviation of the original population. From (3.2), we note that as increasing the sample size by including more elements, the standard deviation of the median tends to diminish by the factor of $\sqrt{\text{N}}$. This explains the linearity improvements after δ passes the theoretical limit of 27%. The same property holds for all ordered elements in which their error standard deviations keep reducing by increasing the sample size. Then, we can use this to explain the phenomenon in Figure 3.3, where the overall standard deviations drop every time as increasing δ. From these observations, we can obtain another statement such that a single

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OEM iteration roughly reduces the error standard deviations by a factor of $\sqrt{2}$ while doubling the sample size. This fact was actually shown in Figure 2.2 and 2.3.

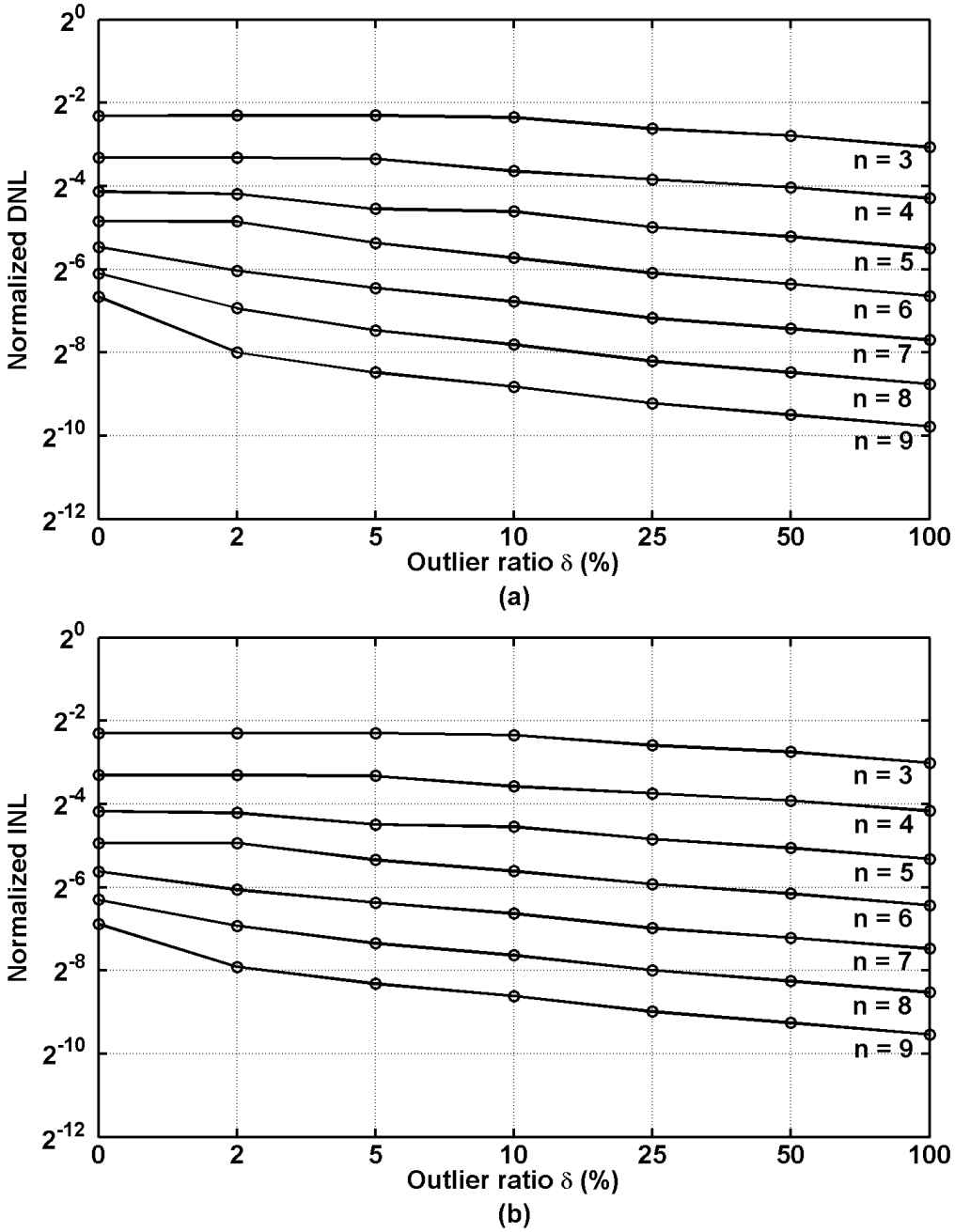

Figure 3.4 Normalized (a) DNL and (b) INL after OEM binarization and outlier elimination with different resolutions of element array and outlier ratios

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3.3 DAC architecture

3.3.1 General considerations

In order to demonstrate the significant linearity enhancements on silicon, we design a 15-bit current-steering DAC with 7-8 segmentation as shown in Figure 3.5. The 7-bit MSB array has the unary-weighted structure. For the optimal outlier elimination as suggested in Figure 3.4, 10% additional elements are included to achieve the best tradeoff between linearity performance and overhead. This would give a total number of 140; however, 144 unit current sources are used in the MSB array to form a 12×12 matrix. Then, according to the grouping information from OEM binarization and outlier elimination, only 127 of the current sources are decoded in a binary-weighted array with the help of some digital circuits. On the other hand, the 8-bit LSB array is made of the conventional binary-weighted structure. Therefore, the 15-bit DAC is operating as a binary-weighted one, and Figure 3.6 illustrates the unit current cell design.

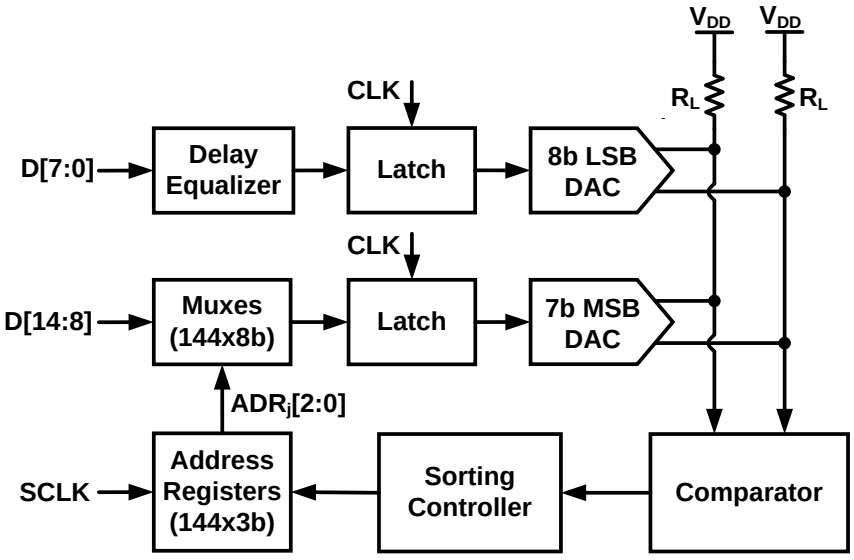

Figure 3.5 15-bit binary-weighted DAC architecture

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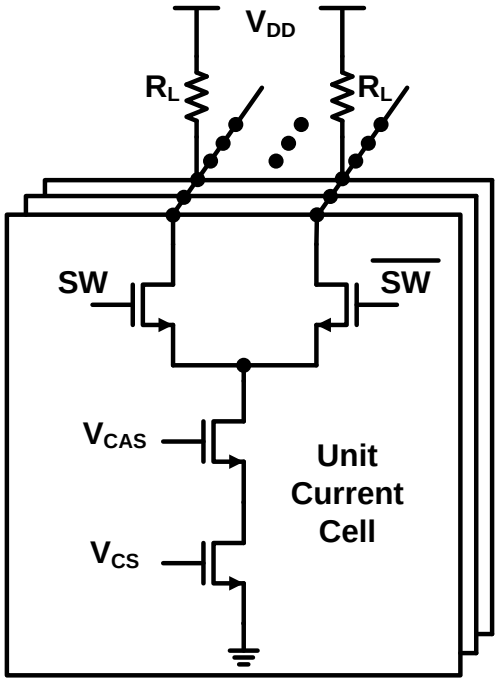

Figure 3.6 Schematic of the unit current cell

If the design target is to achieve INL $\leq$ 0.5LSB with a yield of 99.7%, the relative standard deviation of the LSB current source has to be no larger than 0.15% for a 15-bit binary-weighted DAC. With the new matching techniques, the stringent matching requirement can be relaxed significantly. In this specific case, we will allocate half of the error budget between the MSB and LSB arrays. Based on Monte Carlo simulations, the relative standard deviations of the unit current source within the two segments are 0.42% and 0.84%, respectively. To be more instructive, the current source area reduction factor is around 1400! Table 3.1 summarizes the current source gate area allocations for different segments.

Besides the random errors, systematic errors can also cause nonlinearity. Some special techniques are used to ensure they are within acceptable levels.

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- All the current sources are made of cascoded structures to ensure they have sufficiently high output impedance.
- Each unit MSB current source is divided into 4 subunits, and common centroid layout is applied. Moreover, two rows and columns of dummy current cells are used to surround the main current source matrix for minimizing edge effects [13]. The MSB layout floorplan is shown in Figure 3.7.
- Wide ground wires are used for the current sources to reduce gradient errors due to the ground resistance.
- Bias voltage calibration is applied to the 8-bit LSB array to compensate the inter-segment gain errors, which cause large jumps during the LSB to MSB transitions as shown in Figure 3.8. The bias voltage will be tuned to ensure the average MSB current is equal to 2^8 multiplying by the LSB current. A detailed on-chip implementation can be found in [17].

Table 3.1 Current source gate area allocations for different segments

Segments	Current sources	Gate area (μm^2)
MSB array	MSB unit	32
LSB array	LSB 8	1024
	LSB 7	512
	LSB 6	256
	LSB 5	128
	LSB 4	64
	LSB 3	32
	LSB 2	16
	LSB 1	8

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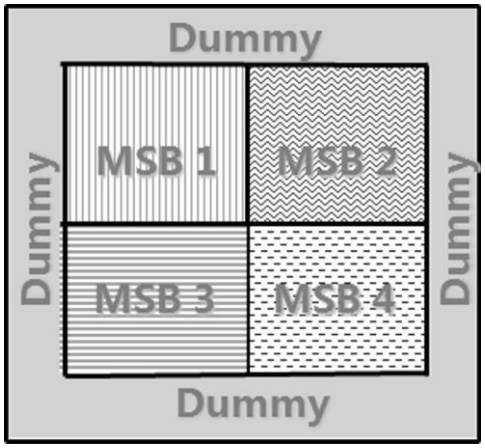

Figure 3.7 Layout floorplan for the 7-bit MSB DAC

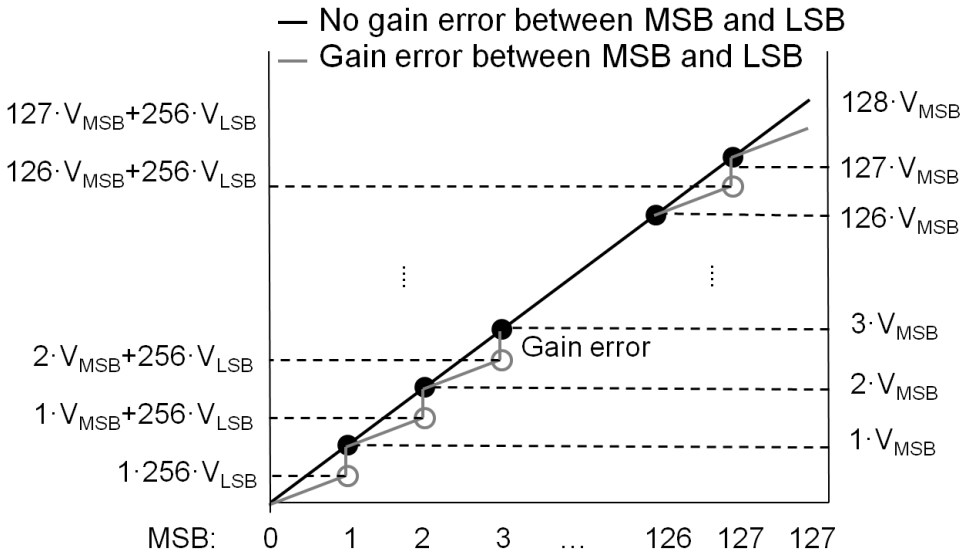

Figure 3.8 DAC transfer curves with and without inter-segment gain errors between the MSB and LSB arrays

3.3.2 Digital circuitry implementations

To realize both OEM binarization and outlier elimination, two key functions need to be allowed. One is to rank all the unit MSB current sources, while the other one is to identify each current source to the appropriate groups based on the binarization

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results. Since [18] has already proposed an on-chip solution for ranking current sources, we will not repeat the circuits here but replace them with off-chip electronics and a FPGA board. It should be pointed out that the digital sorting controller would be much simpler here because of the binary-weighted operation if an on-chip solution is desired.

Each current source can end up with anyone of the (n+1)-bit input lines, i.e., the actual n-bit input plus one extra bit to indicate outlier throwaway. This requires, for each current source, an (n+1)-to-1 digital multiplexer and a $\log_2$(n+1)-bit D flip-flop to store the corresponding address code to indicate the final element destination. Since the total number of the MSB unit current sources is 144 in this work, 144 8-to-1 multiplexers and 144 3-bit D flip-flops are demanded. Figure 3.9 illustrates the detailed circuit blocks of the 7-bit MSB array.

As shown in Figure 3.9, the 144 D flip-flops are connected in a daisy chain where the inputs of the preceding ones come from the outputs of the succeeding ones. Equivalently, the system can be viewed as a serial-in parallel-out shift register. Then, 144 address codes can be sequentially loaded into the DAC. Table 3.2 shows the corresponding address code and the number of current sources for different bit lines during the normal conversion phase. For example, 64 out of 144 current sources belong to the highest bit D[14] with address codes “111”, and thus they are controlled simultaneously based on the code assigned to D[14]. The same idea can be applied to any other bit lines. It is worth mentioning that address codes “000” correspond to the outliers that are banned to use during the DAC normal conversion time. With such arrangements, the 7-bit MSB DAC will operate in a binary-weighted manner.

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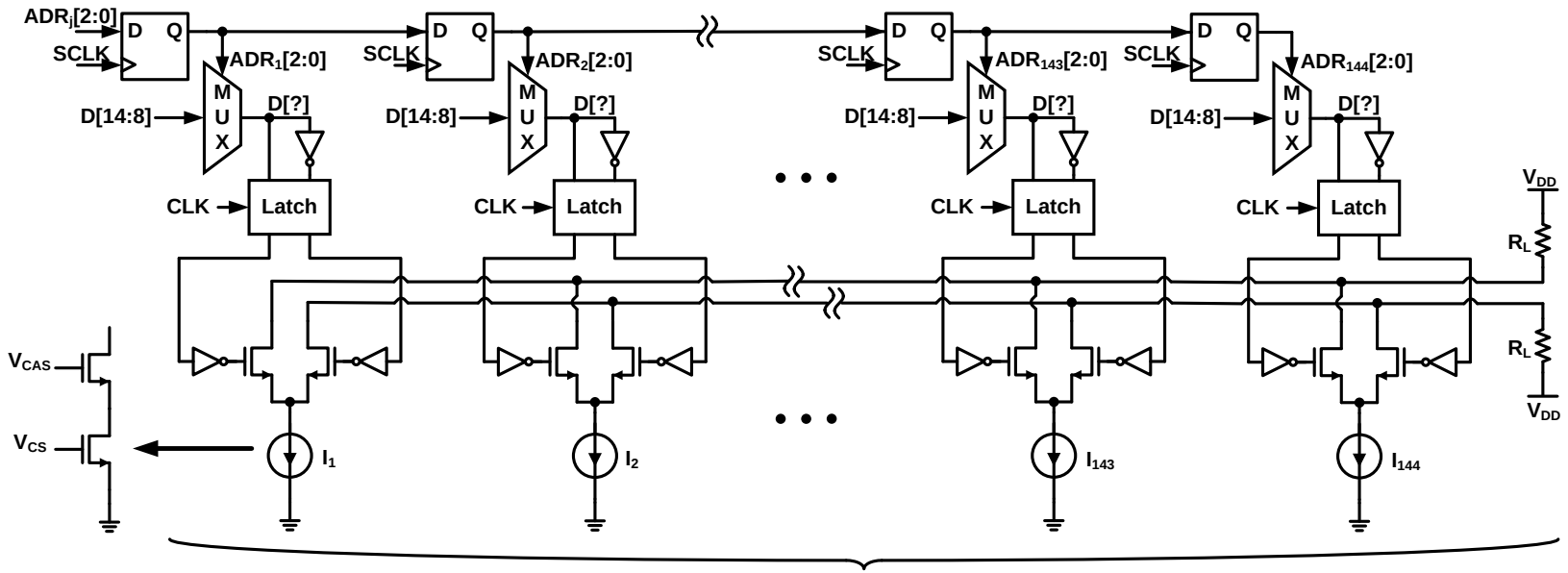

Figure 3.9 Circuit implementation of 7-bit MSB array

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Table 3.2 Address code mapping during normal conversion phase

Address code	Number of elements	Digital input lines
000	17	Don't Care
001	1	D[8]
010	2	D[9]
011	4	D[10]
100	8	D[11]
101	16	D[12]
110	32	D[13]
111	64	D[14]

Table 3.3 Address code mapping during comparison phase

Address code	Number of elements	Digital input lines
001	k^a	D[8]
010	k^a	D[9]
110	$72\text{-}k^a$	D[13]
111	$72\text{-}k^a$	D[14]

[a]The variable k depends on the stages of OEM iterations, where k = 1, 2, 4, 8, 16, and 32.

3.3.3 Current source comparison

While in the current source comparison phase, 144 specific address codes will be loaded. To be more instructive, a variable k is introduced here. The address codes to the 144 current sources and the corresponding digital bit lines are shown in Table 3.3. Our goal is to compare the current sources with address code 001 to those with 010. The variable k is determined by the stages of OEM operations. Based on the theory, we need 6 OEM iterations in order to generate 7 binary-weighted current sources out of the 144 unit current sources. Thus, k can be set to 1, 2, 4, 8, 16, and 32.

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Suppose that we are at the first time OEM iteration, then k = 1. We set D[8] and D[9] to be 1 and 0, respectively. D[13] and D[14] are assigned to 1 and 0, respectively. Furthermore, all the other digital input bits are 0. From this setup, each output side will have 72 MSB current sources flowing. Then, the resulting differential current output can be stored. Followed by that, we will adjust D[8] and D[9] to be 0 and 1, respectively, and keep all the other inputs as the same as before. Consequently, we have swapped the output sides for the current sources with address codes 001 and 010. Subtracting the previously stored differential value from the present one, we can have current difference doubled between the comparing current sources, thus obtaining the relative ranks. This process can be repeated for any other current sources at any stages of OEM iterations. Therefore, the complete current source orders can be easily attained by an efficient merge-sort algorithm implemented on the FPGA.

It should be pointed out that the described operation above is similar to the on-chip implementation shown in [18] but with different digital control mechanisms. Therefore, their current comparator can be directly used in our case. Furthermore, thanks to the binary-weighted operation, the sorting controller can be much simpler here since there are only 7 possible MSB routing address codes and it requires no thermometer decoder.

3.4 Board design

The 15-bit binary-weighted current-steering DAC is implemented in a 130nm digital CMOS process with 1.2V supply voltage. The full-scale current is 5mA driving

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either external 50Ω load resistors or transformers directly. Figure 3.10 shows the die photograph of the chip. The active area is less than 0.42mm^2, among which the 7-bit MSB current source area is well within 0.021mm^2.

The chip is available in a 52-pin QFN package. Figure 3.11 illustrates the chip's bonding diagram, while Table 3.4 describes the functionalities of all the terminals. In order to interact with the chip, we need to provide power supplies, bias current inputs, digital data inputs, clock interface, and output configuration.

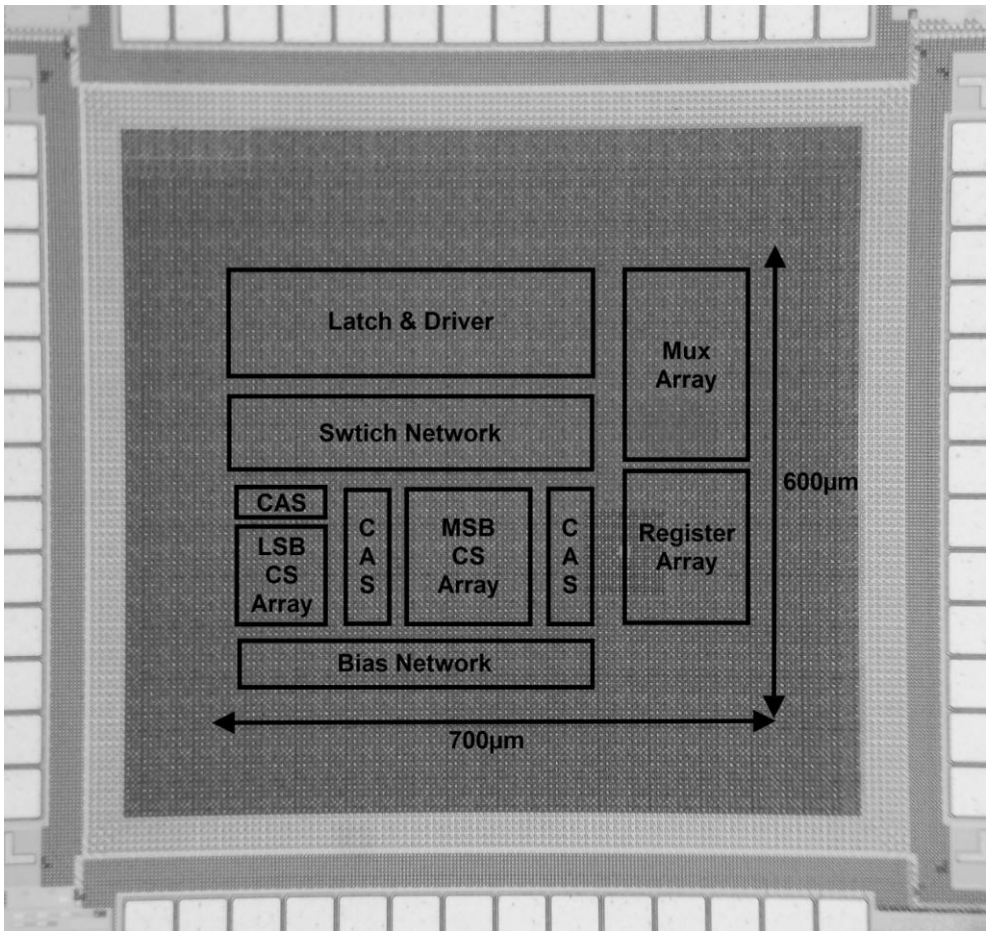

Figure 3.10 Die photograph of the chip

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3.4.1 Power supplies

It is important to give clean and stable power supplies to the DAC. Direct power sources (Agilent E3631A) are used for this purpose. Meanwhile, the analog, digital and clock sections of the board will use the separate supply sources. It prevents the noisy signals to interrupt with the quiet analog signals. Additional bypass capacitors and ferrite beads are applied when the power supplies travel to the board and to the chip's terminals. By doing so, high frequency noise can be suppressed. Power plane is not used here since the routes to the power terminals are all simple, and the associated currents are small.

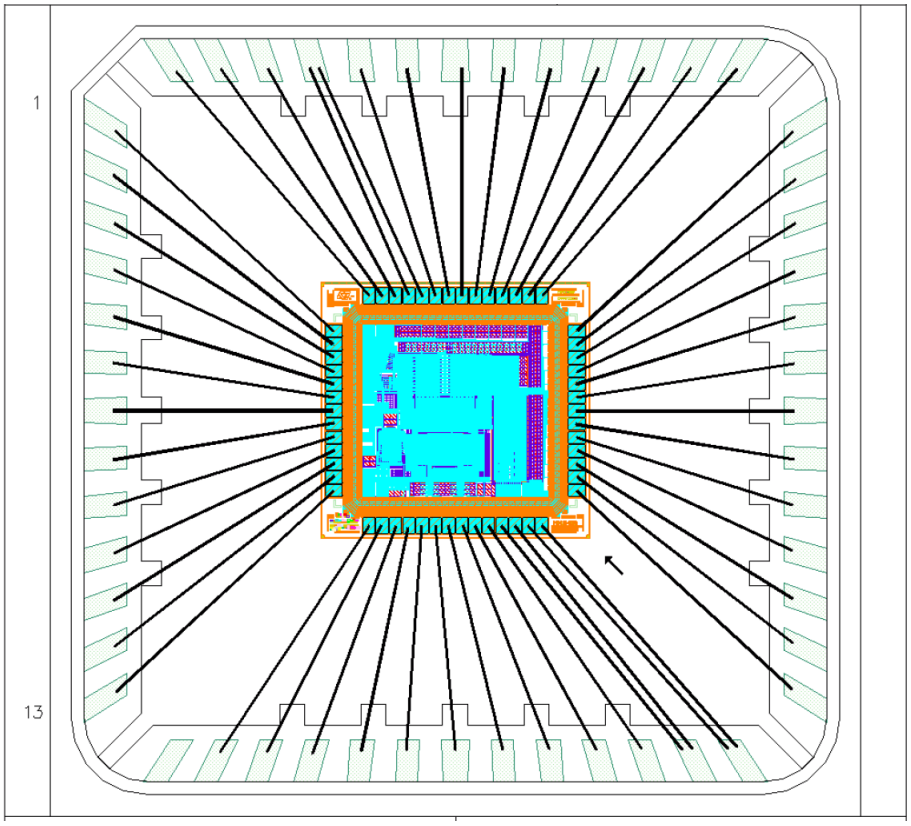

Figure 3.11 Chip bonding diagram

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Table 3.4 Chip terminal functions

Terminal		Type	Description
Name	NO.		
DGND	1, 3, 12, 25, 51	Power	Digital ground return for the internal digital circuitry.
DVDD	2, 13, 24, 26, 52	Power	Digital supply voltage for the internal digital circuitry (1.2V).
VL	4	Power	Low supply voltage for the DAC's switch buffers.
VH	5	Power	High supply voltage for the DAC's switch buffers.
AGND	6, 16	Power	Analog ground return for the internal analog circuitry.
VLD	7	Power	Low supply voltage for the linearization DAC's switch buffers.
VHD	8	Power	High supply voltage for the linearization DAC's switch buffers.
$IOUT_P$	9	Output	DAC current output.
$IOUT_N$	10	Output	Complementary DAC current output
$VCAS_{LSB}$	11	Input	Bias input for the cascode transistors in the 8-bit LSB DAC.
AVDD	15	Power	Analog supply voltage for the internal analog circuitry (1.2V).
VCS_{LSB}	17	Input	Bias input for the current source transistors in the 8-bit LSB DAC.
$VCAS_{MSB}$	18, 19, 21, 22	Input	Bias inputs for the cascode transistors in the 7-bit MSB DAC.
VCS_{MSB}	20	Input	Bias inputs for the current source transistors in the 7-bit MSB DAC.
VCS_{LIN}	23	Input	Bias inputs for the current source transistors in the linearization DAC.
EN_B	27	Input	Active low. Enable data written to the D flip-flop array.
RST_B	28	Input	Active low. Reset the D flip-flop array.
CLK_{CAL}	29	Input	Positive-edge triggered. Clock input for the D flip-flop array.
ADR[2:0]	[30:32]	Input	Data inputs for the D flip-flop array.
D[15:9]	[33:39]	Input	Data inputs for the 7-bit MSB DAC.
DX	40	Input	Don't care. Extra data bit indicating outliers.
D[1:8]	[41:48]	Input	Data inputs for the 8-bit LSB DAC.
CLK	49, 50	Input	Clock inputs during the DAC's normal conversion time.

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To provide quick ground current returns when analog, digital and clock sections communicate, all the grounds will join together at the DAC. Furthermore, a solid ground plane is applied to minimize the inductance due to the ground loop. For the best practice, a split ground plane is started for the analog, digital, and clock signals. Then, the ground plane is connected via 0-ohm resistors. In such arrangements, the signal return currents can flow next to the signal traces with the minimum path impedance.

3.4.2 Bias current inputs

Sufficient bias currents are required for the current source and cascode transistors in the MSB and LSB arrays. Here, an on-board voltage reference is used to generate the bias currents with the help of high precision amplifiers. Figure 3.12 illustrates the schematic of a low noise current source. R_{SET} can be partially tunable so that the desired operating points can be obtained with minor adjustments. It should be noted that proper current mirrors are applied on board to generate multiple current copies with high precision transistor networks. Meanwhile, the bias inputs are made of thick trace lines to minimize the voltage drops.

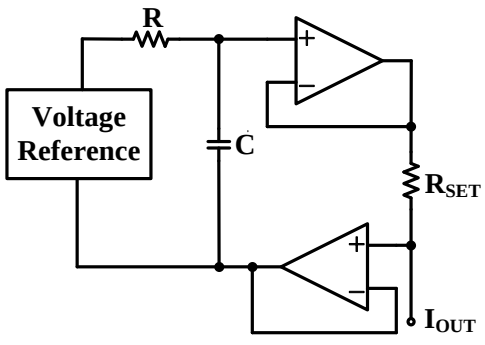

Figure 3.12 Schematic of a low noise current source

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3.4.3 Digital data inputs

The digital data inputs (D[1:15]) are provided by Lattice ECP3 Versa board. The board's output levels are 3.3V; however, the DAC's input voltage compliance range is only around 1.2V. Therefore, a 3.3V-to-1.2V level translator has to be inserted on our board between the FPGA and DAC. In this case, we use a 16-bit edge-triggered D flip-flop (SN74AUC16374) that is able to handle 3.3V digital inputs and generate 1.2V outputs. Another reason for using this chip is that the 15-bit data can be aligned by the clock signal before going into the DAC. Furthermore, all the digital lines need to have exactly the same length for the same delays, and they are designed with 50Ω characteristic impedance.

The other digital inputs such as EN_B, RST_B, CLK_{CAL} and ADR[2:0] are at much lower operation speed. Thus, they are not as critical as the 15-bit inputs, but a buffer (SN74AUC16244) is still needed to translate the voltage level from 3.3V to 1.2V. Meanwhile, 22Ω resistors are connected in series with all the digital lines for signal integrity purposes.

3.4.4 Clock interface

Depending on the speed and performance targets, clock performance can be critical. For low speed operations, we use the clock source provided by the FPGA board directly. On the other hand, the high speed operation requires good jitter performance, and thus we use a precision clock conditioning board (LMK04002BEVAL) to satisfy the criteria. Since we need to supply clock signals for both of the DAC and 16-bit edge

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triggered D flip-flop, a clock distributor chip (LMK00105) is used on board. The chip is powered with a 3.3V DC source, and a resistor divider is used for the clock path to the DAC to meet the input compliance range. Figure 3.13 and 3.14 show the clock setups for the DAC's low and high speed operations, respectively. It should be noted that the clock signals after the distribution chip should have the same delays as the 15-bit data lines after the D flip-flop. Furthermore, the single-ended clock lines are terminated with 50Ω resistors, while the differential lines are terminated with 100Ω resistors.

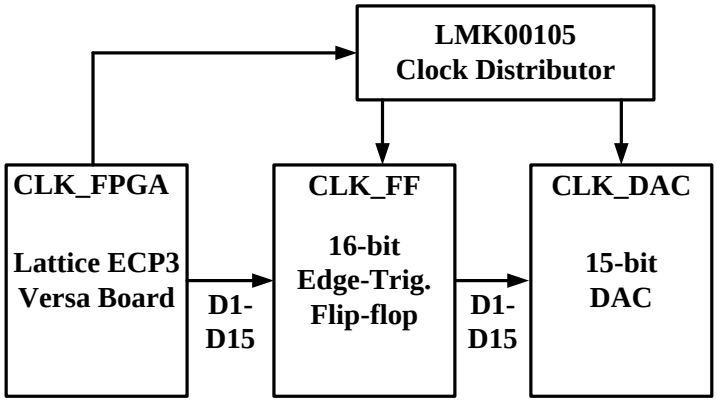

Figure 3.13 Clock setup for the DAC's low speed operations

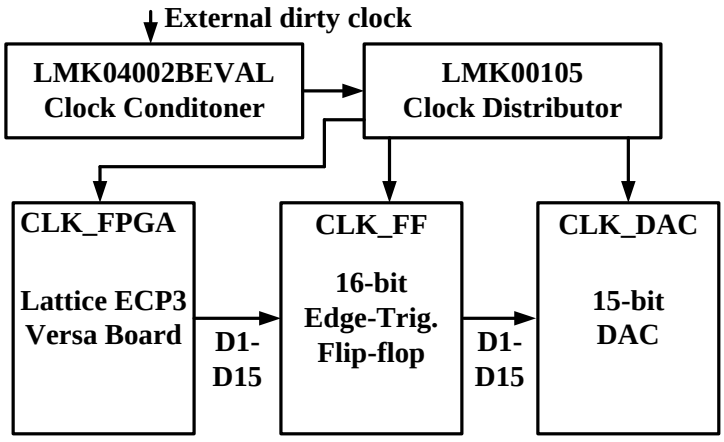

Figure 3.14 Clock setup for the DAC's high speed operations

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3.4.5 Output configuration

To achieve the best DAC performance, it is critical to set the correct output DC bias levels with the desired impedance loads. For static performance tests, two external 50Ω resistors are directly connected to the DAC's complementary outputs in series with 1.2V power supply voltages as illustrated in Figure 3.15. This will generate a peak-to-peak differential voltage of 0.5V with 5mA full-scale current. Then, a high precision ADC board (ADS1259EVM-PDK) or digital multimeter (Agilent 3458A) can be used to measure the DAC's outputs.

For dynamic performance tests, a transformer with an impedance ratio of 4:1 is connected to the differential DAC outputs as shown in Figure 3.16. It converts the fully differential signals to a single-ended signal which will be sent to a spectrum analyzer with a 50Ω resistor load. The middle point of the primary turn of the transformer is connected to a 25Ω resistor in series with the 1.2V power supply voltage. By doing so, a DC path is created to let the current flow. Furthermore, it ensures that the output voltages are within the compliance range. The 50Ω load resistance will be transformed to 200Ω by the impedance ratio from the secondary side to the primary side. Taking that with two 100Ω resistors in parallel, the equivalent AC resistance is still 50Ω on the single output side. Therefore, the differential peak-to-peak voltage level is still 0.5V; however, since the voltage ratio is 2:1 for the 4:1 impedance ratio transformer, the equivalent single-ended voltage on the secondary side will be halved, which generates a 0.25V peak-to-peak signal. The differential output signals are routed differentially so that they experience the same feedthrough and thermal gradient errors.

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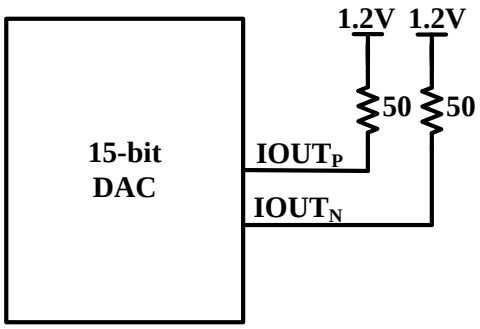

Figure 3.15 Output configuration for the DAC's static performance tests

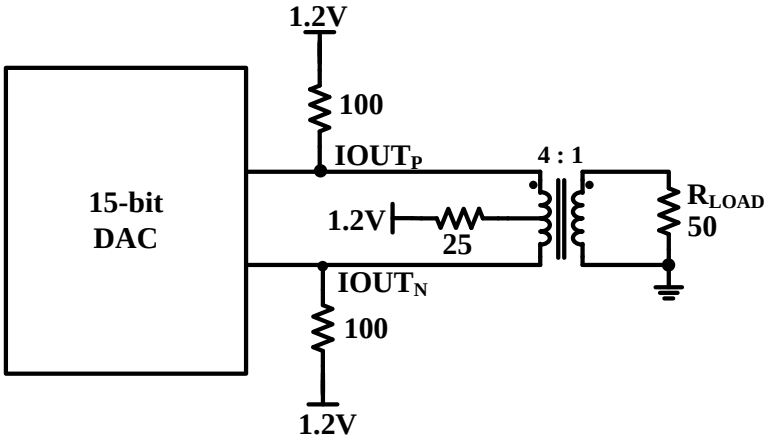

Figure 3.16 Output configuration for the DAC's dynamic performance tests

3.4.6 Board overview

Overall, the printing circuit board (PCB) contains 4 layers due to the characteristic impedance requirements. Layer 1 and 4 are for main signal routings, while layer 2 and 3 are ground planes. With this arrangement, the ground return loops can be well controlled. Layer 3 is usually used as the power plane; however, in our case, the power routings are quite easy and the associated current is small as mentioned before, and therefore thick trace lines are implemented for power lines. Figure 3.17 shows the photograph of the final PCB,

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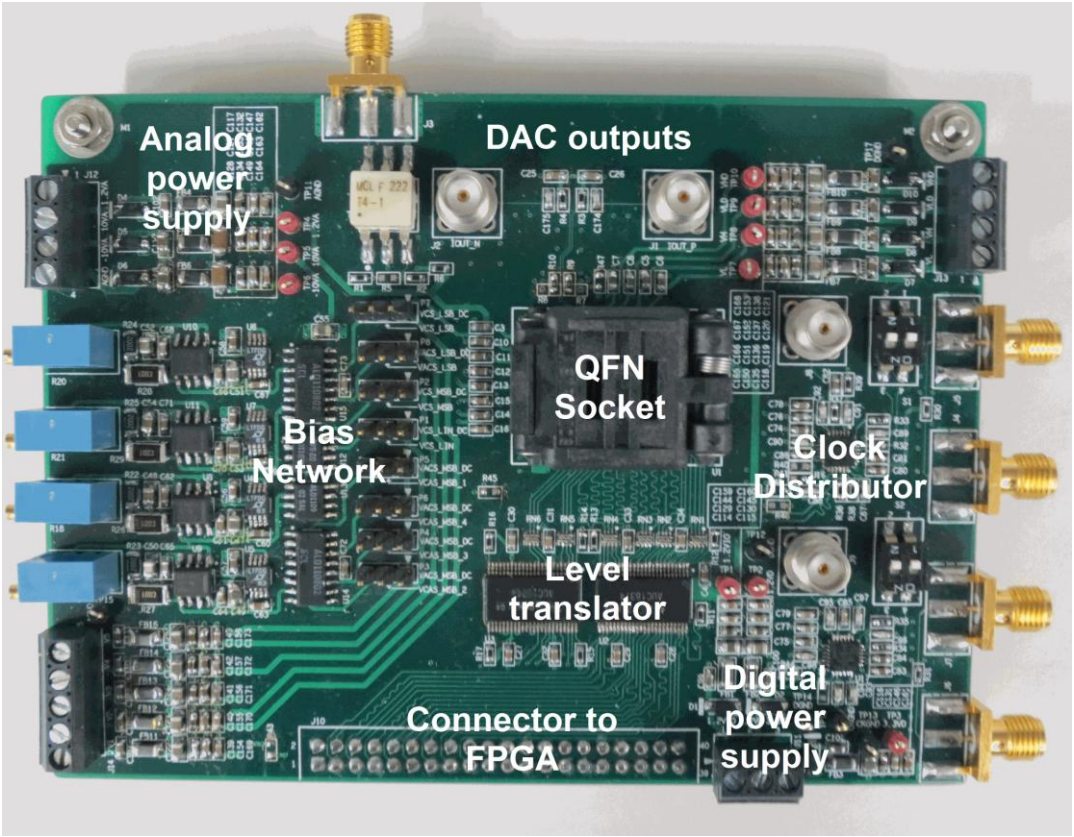

Figure 3.17 Photograph of testing PCB

In order to achieve 15-bit performance, everything needs to be carefully designed. Due to the lack of experience, two rounds of PCB are fabricated. The following list includes some advice based on the mistakes and inconvenience from the first PCB design. This can prevent others to repeat the same mistakes.

- Select parts carefully based on the dimensions, ratings, usability and price.
- Be aware of part orientations which may cause inconvenience during testing.
- Make sure that the parts' footprints exactly match the ones in the data sheets.
- Draw a good floorplan before the PCB layout, and consult with experienced PCB designers to oversee any issues.

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- Use sockets for the chip under test if many chips need to be measured. This saves the effort and time to solder packages such as QFN, but the speed may be affected depending on the socket quality.
- Take care of the synchronizations between digital input and clock signals.
- Design the high speed trace lines with appropriate characteristic impedance, i.e., 50Ω for single-ended lines and 100Ω for fully differential lines.
- Route DAC's complementary outputs differentially to minimize offset errors.
- Place bypass capacitors to the device under test as closely as possible.

Even though a great deal of time has been spent, the high speed performance is still not as good as expected. There are many things that need to be optimized on the board design. However, a major bottleneck for us is that CMOS data transmitting is used on board instead of differential signaling such as LVDS and CML. With all the parasitic capacitance, the digital input and clock signals are not well preserved. This is something that we need to take care of for the next chip fabrication.

3.5 Measurement results

With random binary group assignments to the 144 MSB unit current sources, the DAC's DNL and INL are 9.85LSB and 17.41LSB, respectively. However, after loading address codes obtained by OEM binarization and outlier elimination, the DNL and INL can be reduced to 0.34LSB and 0.77LSB, respectively. Figure 3.18 plots the static linearity performance before and after the new matching techniques.

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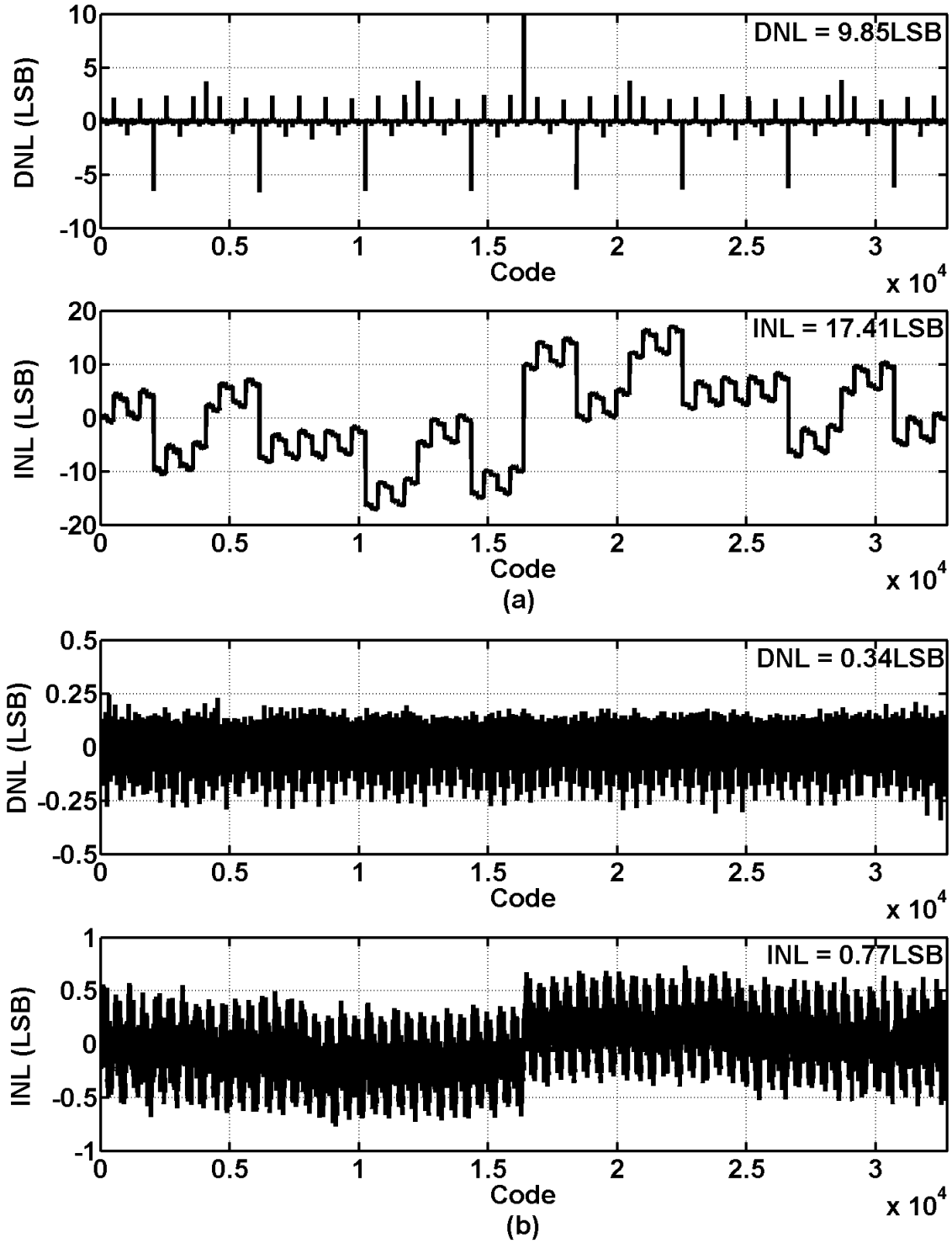

Figure 3.18 Static linearity performance of the 15-bit binary-weighted DAC (a) before and (b) after OEM binarization and outlier elimination

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Table 3.5 shows the matching performance advancements compared to state-of-the-art techniques, e.g., [17] and [18]. Since we did not implement the sorting controller on chip, the area is taken out of the total chip area for [18] to maintain a fair comparison. On the other hand, the current comparator is so small that it does not affect the overall area consumption. Meanwhile, it is worth mentioning that the authors in [17] did not account for the area of 16-bit sigma-delta ADC.

Figure 3.19 shows the measured DAC's output spectrum performance before and after OEM binarization and outlier elimination with 0.4MHz signal frequency and 10MHz sampling frequency. The SFDR can be increased from 67dB to 84dB.

Table 3.5 Matching performance comparison with state of the art

Specifications	Self-Cal. [17]	SSPA [18]	OEM Binarization
Resolution	14-bit	14-bit	15-bit
Structure	6b Unary MSB 8b Binary LSB	7b Unary MSB 7b Binary LSB	7b Binary MSB 8b Binary LSB
Technique	Calibrate MSB current values	Adjust MSB switching sequence	Regroup MSB current sources
Process	CMOS 130nm	CMOS 180nm	CMOS 130nm
Power supply	1.5V	1.8V	1.2V
Full current	10mA	16mA	5mA
DNL	5LSB (before) 0.34LSB (after)	0.63LSB (before) 0.56LSB (after)	9.85LSB (before) 0.34LSB (after)
INL	9LSB (before) 0.43LSB (after)	1.37LSB (before) 0.76LSB (after)	17.41LSB (before) 0.77LSB (after)
Area	$0.1mm^{2}$ [a]	$2mm^{2}$ [b]	$0.42mm^{2}$

[a]The area of 16-bit sigma-delta ADC was not taken into account.
[b]The area of sorting controller is taken out of the total chip area.

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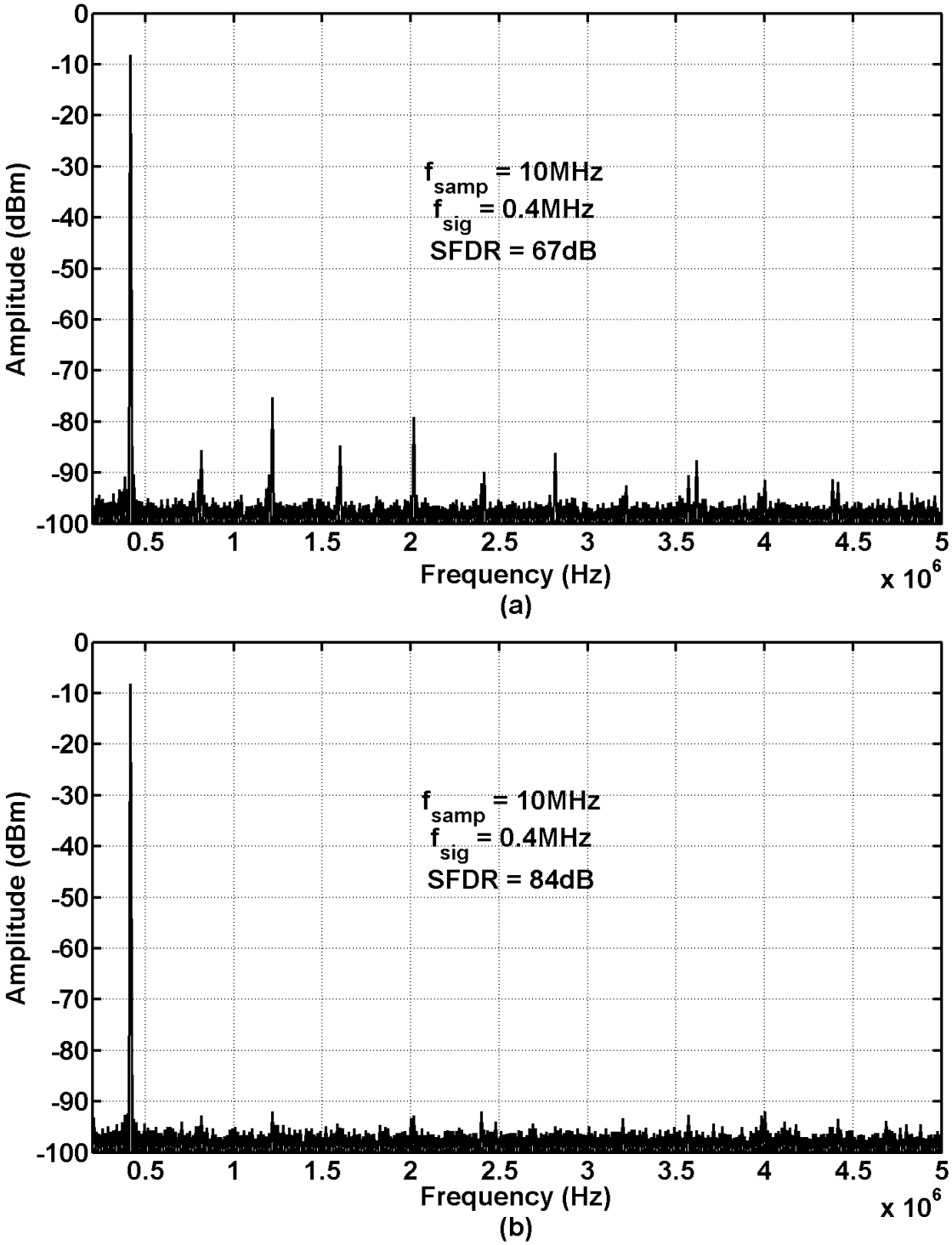

Figure 3.19 Output spectrum of the 15-bit binary-weighted DAC (a) before and (b) after OEM iterations with f_{samp} = 10MHz and f_{sig} = 0.4MHz

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The SFDR versus input frequencies at the 10MHz sampling frequency is shown in Figure 3.20. As we can see, the SFDR performance quickly falls off while increasing the frequencies. This is because that many error sources that cause high frequency nonlinearities were not taken into account during the design phase, e.g., timing errors. Furthermore, lack of knowledge on high speed PCB designs was another limitation. However, all of these can be taken care of by many existing design techniques such as [45]-[54]. By combining these techniques with the new matching strategies, the high frequency linearity is expected to be extended since the nonlinear parasitic capacitance associated with the large area is greatly reduced.

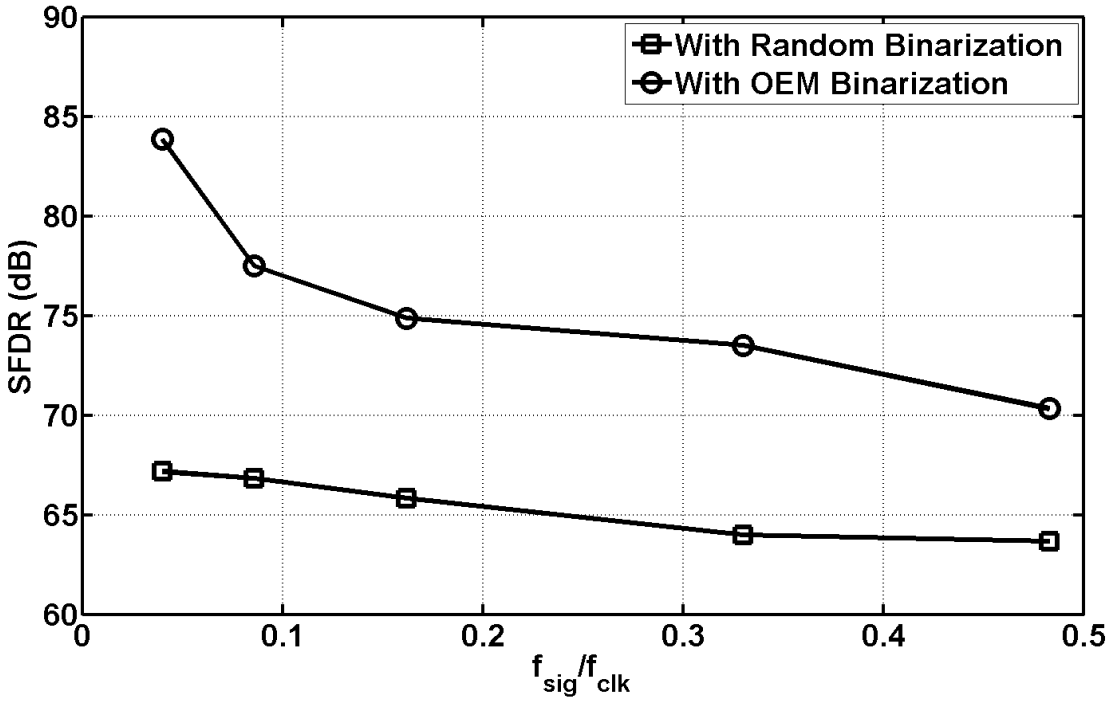

Figure 3.20 SFDR vs. input frequencies at the 10MHz sampling frequency

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3.6 Conclusion

In order to confirm the OEM theory on silicon, a 15-bit binary-weighted current-steering DAC is fabricated in a 1.2V 130nm digital CMOS process. The active area of the chip is less than 0.42mm^2. More importantly, the MSB current source area is well within 0.021mm^2. Experimental results have shown that the DAC's DNL and INL can be both reduced significantly. The new matching techniques only demand the component orders, thus requiring a comparator and some digital circuitry. Such implementation scales well with IC technologies, which may offer one alternative solution to random mismatch errors in the variability-excessive processes.

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CHAPTER 4

NEAR-OPTIMAL BINARIZATION AND SEGMENTATION FOR DATA CONVERTER DESIGNS

4.1 Introduction

In Chapter 2 and 3, we proposed OEM binarization and outlier elimination, and demonstrated the ideas on a high-resolution and high-linearity DAC design. It proves that correct interconnection and combination from a population of elements with significant variability can produce an effective system level matching. On the other hand, it raises the question of whether the binarization strategy is optimal in terms of the complexity and matching performance.

Furthermore, the new matching strategies still require careful considerations of a tradeoff between resource and performance. It is because that the associated design complexity grows exponentially and becomes practically difficult as the resolution bits increase. The same issue happens for many high-resolution data converters regardless of the implementation details [10], [14], [16]-[19], [55]-[60]. A general solution is to use segmented structures. For various circuit implementations, different segmentation strategies [45], [61]-[63] may be required to achieve the optimal tradeoff. A systematic study on how to segment, i.e., the number of segments, the number of bits in each segment, and the resource allocation between segments will be extremely valuable in assisting the circuit designers. Moreover, this study could lead to a common segmentation approach to any data converters with given design techniques and their

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associated implementation details.

This chapter is organized as follows. In Section 4.2, the binarization problem in a population of unit elements is formally set up, and different heuristic solutions are proposed since the problem is believed to be NP-hard. Then, MATLAB simulation results show the achieved matching performance by different heuristic methods. OEM binarization features the least complexity and achieves the similar matching performance compared to the others. In Section 4.3, we use the implementation details from Chapter 3 to formulate multiple optimal segmentation problems for OEM binarization, each of which contains an emphasis corresponding to a different design scenario. These optimization problems belong to mixed-integer nonlinear programming. Solving them is awfully hard [64], [65]. A simple but effective heuristic approach to one of the posed problems is presented, which uses a segmented binarization strategy to achieve a near-optimal tradeoff between resource and linearity performance. To explain the heuristic optimization process, we use a 14-bit binary-weighted current-steering DAC design as an example. Following the approach, we provide near-optimal segmentation solutions for a variety of data converters' resolutions. Finally, Section 4.4 concludes this chapter.

4.2 Near-optimal binarization

OEM binarization and outlier elimination show great advantages in the matching performance improvements. However, they only represent one way of reorganizing the unit elements in a population. There are many other binary grouping strategies that perhaps offer better matching performance. In this section, we will thoroughly study the

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binarization problem and different heuristic methods.

4.2.1 Binarization problem setup

A unary-weighted element array S is given with sample size of $m=2^n-1$. The parameter value of each unit element is defined as x_i ($1 \le i \le m$), and random mismatch is the only considered source of error. All the elements are grouped into n disjoint nonempty subsets S_j ($1 \le j \le n$) with certain cardinality specifications such that:

$$\left|S_j\right| = 2^{j-1}, \tag{4.1}$$

$$\bigcup_{j=1}^{n} S_j = S, \tag{4.2}$$

$$\bigcap_{j=1}^{n} S_j = \varnothing. \tag{4.3}$$

Alternatively speaking, the original n-bit unary-weighted array is converted into an n-bit binary-weighted array. The summed elements associated with each bit have new defined weights w_j, where

$$w_j = \sum_{i=1}^{m} x_i b_{ij}. \tag{4.4}$$

b_{ij} is a binary decision variable matrix that determines the corresponding element group information in each bit j. Because of the subsets' cardinality specifications and disjoint nonempty constraint, we have the following relationships:

$$\sum_{i=1}^{m} b_{ij} = 2^{j-1}, \tag{4.5}$$

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$$\sum_{j=1}^{n} b_{ij} = 1, \tag{4.6}$$

$$b_{ij} \in \{0,1\}. \tag{4.7}$$

Each adjacent bit weight should approximately differ by a factor of 2. The objective is to find an optimal binarization strategy that gives the minimum INL. Here, we will use the end-point fit line method to compute the INL at code D as:

$$\mathrm{INL}_D = \sum_{j=1}^{n} w_j D - D\bar{x}, \tag{4.8}$$

$$\bar{x} = \frac{1}{m}\sum_{i=1}^{m} x_i. \tag{4.9}$$

Then, the INL is defined as:

$$\mathrm{INL} = \mathrm{INL}_D^{\max} = \max\left(\left|\mathrm{INL}_D\right|\right). \tag{4.10}$$

The optimization problem can be properly formulated as follows:

$$\begin{aligned} &\text{minimize} \quad \mathrm{INL} \\ &\text{subject to} \sum_{i=1}^{m} b_{ij} = 2^{j-1}, \ \sum_{j=1}^{n} b_{ij} = 1, \\ &\qquad b_{ij} \in \{0,1\}. \end{aligned} \tag{4.11}$$

The binarization process will be more efficient if we choose the 2^n-1 elements from a bigger population since those largely defected elements can be eliminated. We can redefine the sample size of the original unary-weighted array as

$$m = \left\| (1+\delta) 2^n \right\|, \tag{4.12}$$

where δ is the outlier ratio as defined in Chapter 3 and $0 < \delta < 1$. The mathematical operator $\|\cdots\|$ represents round function. Here, we still want to find an optimal

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binarization strategy that achieves the best linearity performance with the same cardinality constraints; however, not all the elements will be selected in this case. Then, the optimization problem can be reformulated as follows:

$$\begin{aligned} &\text{minimize} \quad \text{INL} \\ &\text{subject to} \sum_{i=1}^{m} b_{ij} = 2^{j-1}, \ \sum_{j=1}^{n} b_{ij} \le 1, \\ &\qquad b_{ij} \in \{0,1\}. \end{aligned} \tag{4.13}$$

4.2.2 Heuristic methods

The optimization problems (4.11) and (4.13) are both NP-hard to solve. It is because that they contain multiple cardinality-constrained subset sum problems which are known to be NP-complete [66]. For example, in order to obtain the MSB, we need to choose 2^{n-1} out of m unit elements so that a minimum INL can be achieved at the end. Therefore, it is impossible to solve the problems with limited computational capacity. Heuristic approaches must be used in this situation.

One of the heuristic approaches proceeds as follows:

1. Measure each unit element
2. Compute the parameter average $\bar{x}$
3. Choose 2^{n-1} unit elements whose summed weight is the closest to $2^{n-1} \cdot \bar{x}$
4. Choose 2^{n-2} unit elements whose summed weight is the closest to $2^{n-2} \cdot \bar{x}$ among the remaining elements
5. Repeat the selection steps until there is only 1 element left.

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The complexities of element measurement and average computation are both the same, i.e., O(m). The complexities of element selections are different in different steps. They depend on the number of selected elements and the total number of elements in the set. However, it is obvious that step 3 consumes the most time since the binomial coefficient is $C(2^n\text{-}1,2^{n-1})$, and thus the complexity goes up extremely fast as n increases. As one can see, this approach will not be practically doable once n is greater than 4.

Another heuristic approach takes the reverse direction as the above one:

1. Measure each unit element
2. Compute the parameter average $\bar{x}$
3. Choose 1 unit elements whose summed weight is the closest to $\bar{x}$
4. Choose 2 unit elements whose the summed weight is the closest to $2 \cdot \bar{x}$ among the remaining elements
5. Repeat the selection steps until there are only 2^{n-1} elements left.

In this case, the most time consuming part is when we are selecting 2^{n-2} elements among the remaining elements. Similarly, we have the running time to be extremely long when n is large. Therefore, it will still not be practically doable once n is greater than 4.

The third heuristic approach is actually the OEM binarization as proposed in Chapter 2, which involves the following steps:

1. Sort all unit elements, and group the median element into bit 1
2. Perform the first OEM iteration which is to pair and sum the complementary ordered elements
3. Resort the new elements, and group the median element into bit 2

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4. Continue with the OEM iterations until there are only 2^{n-1} elements left.

Obviously, the first sorting operation is the most time consuming part in the approach, where the running time is of order O(m ŀogm) if an efficient sorting algorithm is applied, e.g., merge-sort. This solves the impractical issues for higher n values posed by the other two approaches. For example, at n = 7, the complexity order is no less than 1000.

The fourth heuristic approach is an upgraded version of the OEM binarization. The associated steps are summarized as follows:

1. Sort all unit elements, and group the most accurate element to $\bar{x}$ into bit 1
2. Perform the first OEM iteration which is to pair and sum the complementary ordered elements
3. Resort the new elements, and group the most accurate element to $2 \cdot \bar{x}$ into bit 2
4. Continue with the OEM iterations until there are only 2^{n-1} elements left.

The only difference from the third approach is to use the most accurate element instead of the median. The computational complexity is about the same as the previous case, but we need to measure each element here.

If more unit elements are included in the population, we can integrate the outlier elimination strategy. However, it is a little different for the first and second heuristic approaches since we can choose the best groups in a larger population and leave the undesired ones behind. Of course, by putting extra elements, it adds another dimension for the optimization difficulty since we need to decide how many extras to include, which ones to throw away, and how to group for the best performance.

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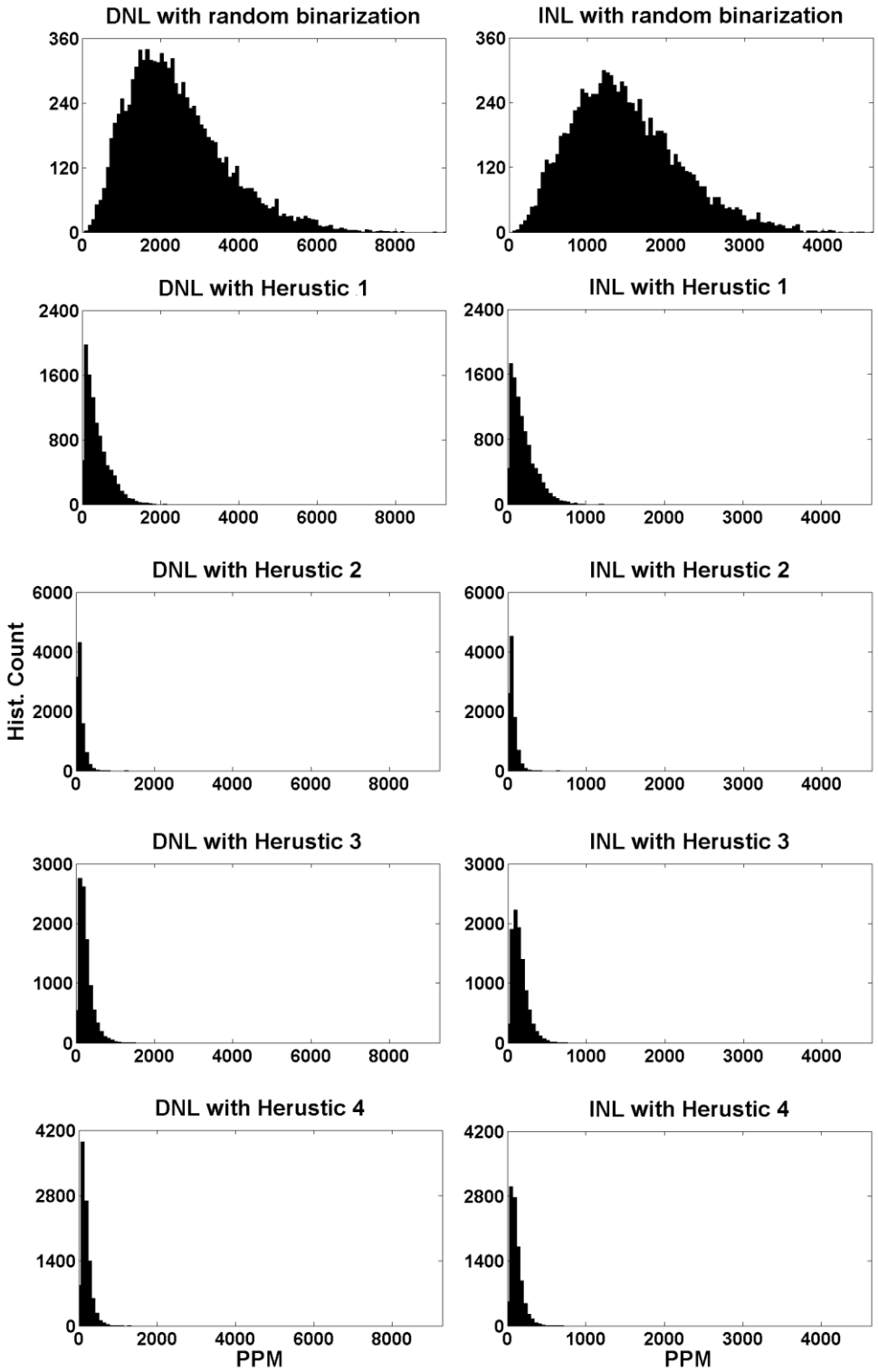

Figure 4.1 DNL and INL distributions of 10,000 randomly generated 4-bit MSB arrays in a 14-bit DAC design after different binarization heuristics

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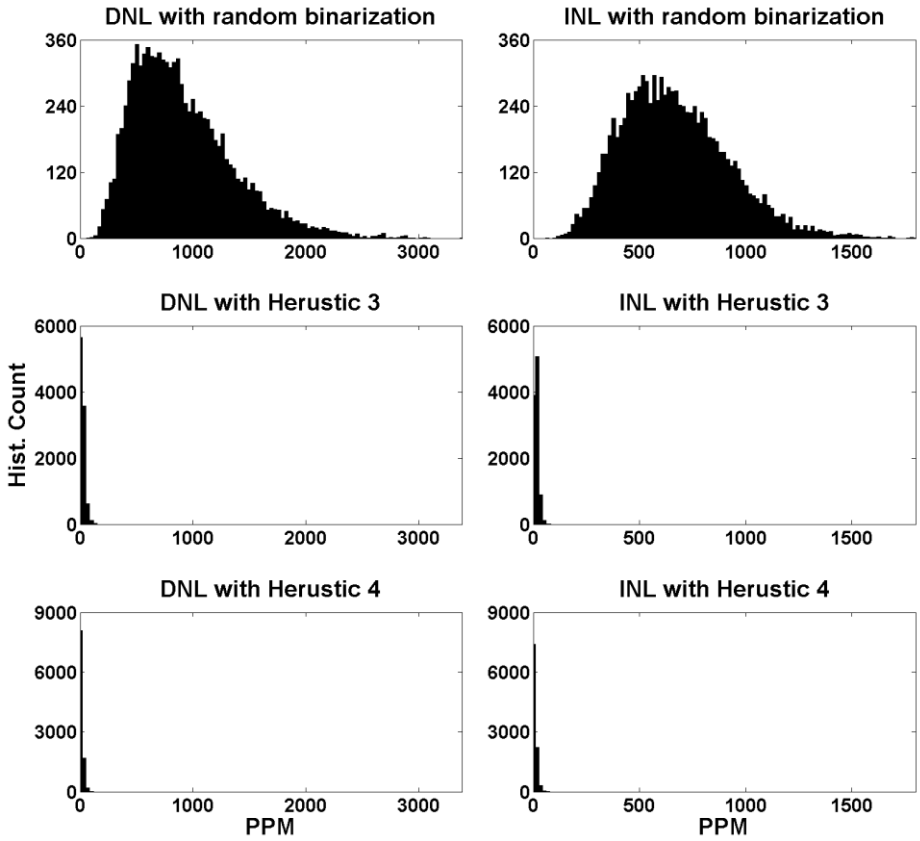

Figure 4.2 DNL and INL distributions of 10,000 randomly generated 7-bit MSB arrays in a 14-bit DAC design after the third and fourth binarization heuristics

4.2.3 Matching performance comparison

In order to compare the linearity performance of these heuristic approaches, we have modeled a 14-bit DAC. Since the first two approaches are hard to simulate when n is larger than 4, we will segment the DAC with 4-bit unary-weighted MSB array and 10-bit binary-weighted LSB array. Then, four different binarization approaches are applied in the 4-bit MSB array. The relative standard deviation of the unit MSB element is chosen to be 1%. After running 10,000 simulations, the MSB DNL and INL performance for different binarization approaches are concluded in Figure 4.1. Furthermore, the original static accuracy by random binarization is also included as a

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reference to compare. Based upon Figure 4.1, we can see that all the heuristic approaches give the same order of magnitude linearity performance, and the second approach achieves slightly better performance than the others. We can also compare the third and fourth heuristics in an array with larger resolution bits, e.g., 7. All the other simulation parameters stay the same as before. Figure 4.2 illustrates that the fourth heuristic is slightly better than the third one.

However, as discussed above, the first and second approaches are not efficient in terms of computational power. Thus, it is not realistic to implement them since the associated hardware design can be a disaster. On the other hand, the third and fourth approaches can be easily implemented. In Chapter 3, we have demonstrated a circuit realization for the third approach using a comparator and some digital circuitry. For the fourth approach, we need to add a measurement mechanism to obtain the most accurate element. This certainly adds one degree of difficulty for the implementation. Therefore, the third approach, i.e., OEM binarization, features simplicity and efficiency in both practical and computational complexity and achieves decent matching performance compared to all the other heuristic approaches. Since the optimal binarization solution is quite difficult to obtain, OEM binarization provides an effective heuristic solution even though it is sub-optimal.

Additionally, outlier elimination can be integrated to improve the matching performance as proven in the previous chapters. In the third and fourth heuristics, we can intentionally include additional number of unit elements and then eliminate both tailed ones after sorting to obtain exactly 2^n-1 elements for the binarization process.

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Adding more elements will also help the first two heuristics, since the selections can be made in a larger population and the undesired ones can be left out at the end, but it is slightly different from the outlier elimination strategy which happens at the beginning of the binarization process. The simulations for the effects of outlier elimination will not be repeated here since we have thoroughly studied them in both Chapters 2 and 3.

4.3 Near-optimal segmentation

To take advantages of the new matching strategies while still consuming a low implementation cost, we need apply segmentation to compromise such situation. In the previous chapters, we gave an arbitrary segmentation and calculated the relative analog area reduction which might not necessarily represent the proper way to achieve the best tradeoff between the overall area and linearity performance. In this section, we will set up multiple versions of optimal segmentation problems with the implementation details given in Chapter 3. Each of the optimization problems will correspond to a different design scenario. Since they are incredibly difficult to solve, we will provide a heuristic approach to one of the problems so that a near-optimal solution can be obtained.

4.3.1 Segmentation problem setup

In an n-bit data converter design, we can establish an independent variable k ($1 \leq k < n$) denoting for the number of segments so that the segmentation allows to change during the optimization process. When k=1, the data converter uses, either a traditional or an OEM based binary-weighted array. Otherwise, it contains both architectures simultaneously. Regardless, we will always have an n-bit binary-weighted structure.

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Each segment may possess different resolutions that can be defined as n_i, where $1 < n_i \leq n$ and $1 \leq i \leq k$. Then, the sum of these variables adds to n:

$$n = \sum_{i=1}^{k} n_i. \tag{4.14}$$

In the following discussions, we will obtain the total required area for the n-bit binary-weighted data converter design, which includes analog area, digital area and other related design area. First, we start the problem setup by defining the required analog area for each segment:

$$\begin{aligned} A_i^{\text{analog}} &= \left\| \left(2^{n_i} - 1\right)\left(1 + \delta_i\right) \right\| A_i^{\text{unit}}, \\ 0 &\leq \delta_i \leq 1, \end{aligned} \tag{4.15}$$

where A_i^{unit} is the analog area of the unit element and δ_i stands for the outlier ratio in segment i. It should be pointed out that the segments implemented by a traditional binary-weighted structure will always have the outlier ratio to be 0. Then, the entire analog area is simply the summation of the analog area from each segment:

$$A^{\text{analog}} = \sum_{i=1}^{k} A_i^{\text{analog}}. \tag{4.16}$$

For the segments realized by OEM binarization and outlier elimination, we need additional digital circuitry. It can be estimated from the given implementation details such that each element requires one D flip-flop and one multiplexer. Then, we have the resolutions of both circuits within each segment as following, where $\lceil \cdots \rceil$ corresponds to ceiling operation.

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$$n_i^{\text{mux}} = \left\{ \begin{array}{l} 1, \text{ Direct binarization} \\ n_i, \ \delta_i = 0, \\ n_i + 1, \ 0 < \delta_i \le 1. \end{array} \right\} \text{ OEM binarization} \tag{4.17}$$

$$n_i^{\text{filpflop}} = \left\{ \begin{array}{l} 0, \text{ Direct binarization} \\ \lceil \log_2 n_i \rceil, \ \delta_i = 0, \\ \lceil \log_2 (n_i + 1) \rceil, \ 0 < \delta_i \le 1. \end{array} \right\} \text{ OEM binarization} \tag{4.18}$$

We can also specify the area of 1-bit D flip-flop and 2-1 multiplexer as A^{flipflop} and A^{mux}, respectively. Since the area of both circuits scales up with their resolutions, we can write the required digital area in segment i with:

$$A_i^{\text{digital}} = \left\| \left(2^{n_i} - 1\right)\left(1 + \delta_i\right) \right\| \left(n_i^{\text{filpflop}} A^{\text{flipflop}} + \left(n_i^{\text{mux}} - 1\right) A^{\text{mux}} \right). \tag{4.19}$$

Followed by this, the total additional digital area can be formulated by:

$$A^{\text{digital}} = \sum_{i=1}^{k} A_i^{\text{digital}} \tag{4.20}$$

Besides, using different sizing strategies among segments may introduce systematic errors, thereby requiring additional k-1 calibration DACs (CALDACs) to compensate the inter-segment errors, e.g., [17]. These CALDACs are applied to the lower segments so that they can be well matched with the upper segments. The area of each CALDAC is proportional to the total area of the corresponding lower segments, where we can write the relationship as follows:

$$\begin{array}{l} A_j^{\text{caldac}} = \alpha_j \sum_{j=1}^{k-1} \left(A_{j+1}^{\text{analog}} + A_{j+1}^{\text{digital}} \right), \\ 0 \le \alpha_j \le 1. \end{array} \tag{4.21}$$

Then, the total area of CALDACs has the similar forms to (4.16) and (4.20):

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$$A^{\text{caldac}} = \sum_{j=1}^{k-1} A_j^{\text{caldac}}. \tag{4.22}$$

Based on everything so far, we can conclude the total estimated design area with:

$$A = A^{\text{analog}} + A^{\text{digital}} + A^{\text{caldac}}. \tag{4.23}$$

From this formulation, we see that the whole area will be only the analog amount if using a conventional binary-weighted array. Alternatively, we will have the integrated digital and CALDAC area on top of the analog area when some segments use OEM binarization. Furthermore, the routing area is not taken into account in (4.23) because our primary goal is to provide a segmentation approach with the best tradeoff between area and linearity performance; however, a more accurate expression for the overall area could be developed if desired.

Next, we will define the DNL and INL performance of the n-bit data converter with a 99.7% yield in the problem setup. They can be written in variables $\mathrm{F}_{\mathrm{DNL}}^{-1}(99.7\%)$ and $\mathrm{F}_{\mathrm{INL}}^{-1}(99.7\%)$, where $\mathrm{F}_{\mathrm{Y}}^{-1}(\mathrm{Q})$ represents the quantile function of the random variable Y when $0 \le \mathrm{Q} \le 1$.

We can impose upper limits on the total area and linearity performance such as:

$$A \le A^{\max}, \tag{4.24}$$

$$F_{\mathrm{DNL}}^{-1}(99.7\%) \le \mathrm{DNL}^{\max}, \tag{4.25}$$

$$F_{\mathrm{INL}}^{-1}(99.7\%) \le \mathrm{INL}^{\max}. \tag{4.26}$$

Alternatively, each variable can be treated as the minimization objective. Then, we can set up different versions of optimization problems, each of which possesses a different

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design emphasis. Table 4.1 gives some examples. More problems can be formulated if we add extra specifications into the setup.

4.3.2 Heuristic approach

Solving the listed optimization problems (4.27)-(4.33) are extremely hard, because all of them belong to mixed-integer nonlinear programming [64], [65]. Instead of chasing after the optimal solutions that might take a long time to determine, we will provide an easy heuristic design approach to one of the posed problems, e.g, (4.27). In this case, we give an INL budget with a 99.7% yield, and want to use the minimum area to create an n-bit binary-weighted data converter. It should be noted that the equivalent heuristic methods can also be developed for other problems.

Table 4.1 Different optimal segmentation problems with each emphasizing on a different design scenario

Objective function (minimize)	Constraints (subject to)	
A	$F_{\mathrm{INL}}^{-1}(99.7\%) \le \mathrm{INL}^{\max}$	(4.27)
	$F_{\mathrm{DNL}}^{-1}(99.7\%) \le \mathrm{DNL}^{\max}$	(4.28)
	$F_{\mathrm{INL}}^{-1}(99.7\%) \le \mathrm{INL}^{\max}$ $F_{\mathrm{DNL}}^{-1}(99.7\%) \le \mathrm{DNL}^{\max}$	(4.29)
$F_{\mathrm{INL}}^{-1}(99.7\%)$	$A \le A^{\max}$	(4.30)
	$A \le A^{\max}$ $F_{\mathrm{DNL}}^{-1}(99.7\%) \le \mathrm{DNL}^{\max}$	(4.31)
$F_{\mathrm{DNL}}^{-1}(99.7\%)$	$A \le A^{\max}$	(4.32)
	$A \le A^{\max}$ $F_{\mathrm{INL}}^{-1}(99.7\%) \le \mathrm{INL}^{\max}$	(4.33)

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The proposed heuristic approach has a near-optimal area and linearity performance tradeoff, and it goes along these steps:

1. Determine the proper uses of OEM binarization and outlier elimination in different resolution cases with given implementation details.
2. Set n_1=3 with predetermined δ_1, and n_2=n–3. Apply OEM and direct binarizations to segment 1 and 2, respectively. Calculate the total area A' needed when both segments contribute to half of the total error budget.
3. Set n_1=n. Apply direct binarization to the n-bit data converter design. Calculate the total area A" needed under the total error budget.
4. Compare A' and A".
    a. If A' ≥ A", one should use a traditional binary-weighted array for the n-bit data converter design (stop here).
    b. If A' < A", one should use OEM binarization within segment 1 (go to step 5).
5. Find the minimum sum of the analog and digital area for segment 1 by using different resolution and outlier ratio cases (obtained from step 1), while the linearity target is within half of the total error budget.
6. Set n_1 to the corresponding resolution where the minimum area sum happens.
7. Change the optimization goal to develop an ($n–n_1$)-bit data converter in the least area with a total error budget being half of the original total error budget.

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8. Repeat steps 2-7 with the new divided optimization problem until we decide all the segmentations.

4.3.3 Design example

To be more informative, we apply the heuristic approach to a design example in which the fabrication technology is a 0.13μm CMOS process with given mismatch parameters A_β=1%·μm and A_{Vt}=4mV·μm, and the goal is to create a 14-bit binary-weighted current-steering DAC for INL ≤ 0.5LSB with a 99.7% yield using the minimum area.

The analog area of the unit current source within each segment can be derived based on the corresponding relative standard deviation $\sigma_i^{unit}/I_i^{unit}$ and overdrive voltage V_{gs}-V_t [28] as follows:

$$A_i^{unit} = \frac{A_\beta^2 + 4A_{V_t}^2 / (V_{gs} - V_t)^2}{2\left(\sigma_i^{unit} / I_i^{unit}\right)^2}. \tag{4.34}$$

The relative standard deviations can be obtained from Monte Carlo simulations while the bias conditions of the unit current sources are all given by V_{gs}-V_t=0.3V for simplicity.

We also provide the standard cell area of 1-bit D flip-flop and 2-1 multiplexer in this technology, where $A^{flipflop}$=34μm^2 and A^{mux}=16μm^2. Furthermore, to simplify the following calculations, we will take α_j in (4.21) to be 1 so that the area of each CALDAC equals to its upper bound, which is the overall area of the corresponding lower segments. Now, all the associated area can be quantitatively evaluated based on the given parameters above.

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Next, we can use the proposed heuristic method to find out the best segmentation for the 14-bit DAC that gives the minimum area within the desired linearity target. The complete steps proceed as following:

Step 1. From Figure 3.4, we have already concluded that the outlier elimination becomes much more effective for the element array whose resolution is greater than 4, and it becomes inefficient after the outlier percentage passes 10% in each case. By increasing the ratio continuously, we will not gain any benefits in this design case since the digital area soon dominates. Furthermore, beyond the 7-bit resolution, the number of multiplexers and flip-flops will become too high which makes the interconnect complexity impractical. Therefore, we should use the new matching strategy with an upper resolution bound of 7. With everything above, we will only consider 5 cases here as summarized in Table 4.2.

Step 2. First, we will set n_1=3, δ_1=0% and n_2=11. From Monte Carlo simulations, to achieve INL $\leq$ 0.25LSB with a 99.7% yield, the relative standard deviations of the unit current source within segment 1 and 2 are 0.0115% and 0.3%, respectively. From those, we can calculate the total area A' as illustrated in Table 4.3.

Step 3. Then, we choose n_1=14. The total area A" is about 1506625μm^2 to achieve INL $\leq$ 0.5LSB with a 99.7% yield if employing a regular binary-weighted array. The standard deviation of the unit current source is 0.21%.

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Table 4.2 Different resolution and outlier ratio cases considered in the heuristic approach based on empirical information

Case #	Resolution	Outlier ratio
1	3	0
2	4	0
3	5	10%
4	6	10%
5	7	10%

Table 4.3 Area calculation in a 14-bit DAC for INL ≤ 0.5LSB with a 99.7% yield using 3-11 segmentation by OEM binarization

14-bit DAC Design	Contributor	Area (μm^2)
Segment 1 3-bit DAC	A_1^{analog}	215361
	$A_1^{digtial}$	700
Segment 2 11-bit DAC	A_2^{analog}	92241
CALDAC 1	A_1^{caldac}	92241
Total DAC	A'	400543

Table 4.4 Minimum area considerations of segment 1 for INL ≤ 0.25LSB with a 99.7% yield using OEM binarization

Cases	Area needed by OEM Binarization		
	A_1^{analog} (μm^2)	$A_1^{digtial}$ (μm^2)	Total (μm^2)
n_1=3, δ_1=0%	215361	700	216061
n_1=4, δ_1=0%	77594	1740	79334
n_1=5, δ_1=10%	19085	6188	25273
n_1=6, δ_1=10%	4477	13662	18139
n_1=7, δ_1=10%	1344	29960	33508

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Step 4. Since A'<A", we should apply OEM binarization.

Step 5. To make most out of the new matching strategy, we can consider the cases listed in Table 4.2 when the linearity goal is INL ≤ 0.25LSB with a 99.7% yield. Based on the calculations in Table 4.4, we will set n_1=6 and δ_1=10%, which gives the minimum total area.

Step 6. After identifying the resolution of segment 1, we will replace the optimization goal to produce an 8-bit DAC for INL < 0.25LSB with a 99.7% yield by the minimum area.

Step 7. Using the similar approach, we can find that OEM binarization will still have area advantage. Thus, we will keep using it.

Step 8. By considering the minimum area sum for segment 2 when the linearity objective is INL ≤ 0.125LSB with a 99.7% yield, we will set n_2=3 and δ_2=0.

Step 9. Once again, we will reformulate the optimization problem to produce a 5-bit DAC for INL ≤ 0.125LSB with a 99.7% yield using the minimum area.

Step 10. From the area comparisons, we can show that a regular binary-weighted array will give the minimum area instead. Therefore, we will set n_3=5.

Consequently, the near-optimal segmentation for the 14-bit DAC is 6-3-5, and the total area is about 20143μm^2. Table 4.5 lists the area occupations from different segments. In contrast, the traditional segmentation strategies such as 6-8 [17] and 7-7

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[18] within the same linearity condition will give the overall area of 23245μm^2 and 32431μm^2, respectively.

We can also apply this heuristic approach to various data converters' resolutions for INL ≤ 0.5LSB with a 99.7% yield. From the same implementation details, Table 4.6 summarizes the near-optimal segmentation solutions. Furthermore, the same optimization process can be applied to any data converter designs. For different implementation details, different optimal segmentations may be required. Therefore, designers will need to set up the optimization problems and implement the heuristic steps illustrated here for their own design cases.

4.4 Conclusion

In this chapter, we raise the question of optimal binarization, and properly set up the problem. Different heuristic solutions are proposed along with a discussion of the associated practical and computational difficulties. Based on these, OEM binarization is proven to be simple and easy to implement, and meanwhile, it achieves the similar matching performance compared to the other binarization methods. In addition, we also provide a segmented binarization strategy to accomplish a near-optimal tradeoff between the area and linearity performance, which enables various applications in high-resolution and high-linearity data converter designs for the new matching strategies. Furthermore, this segmentation approach can be replicated in many other data converter designs regardless of the implementation details.

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Table 4.5 Total area calculation in a 14-bit DAC for INL ≤ 0.5LSB with a 99.7% yield using segmented binarization

14-bit DAC Design	Contributor	Area (μm^2)
Segment 1 6-bit DAC	A_1^{analog}	4477
	$A_1^{digtial}$	13662
Segment 2 3-bit DAC	A_2^{analog}	197
	$A_2^{digtial}$	700
Segment 3 5-bit DAC	A_3^{analog}	70
CALDAC 1	A_1^{caldac}	967
CALDAC 2	A_2^{caldac}	70
Total DAC	A'	20143

Table 4.6 Near-optimal segmentation solutions in various resolution targets for INL ≤ 0.5LSB with a 99.7% yield

Resolution	Optimal segmentation
8	8
10	3-7
12	4-3-5
14	6-3-5
16	7-3-6
18	7-5-6
20	7-6-7

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CHAPTER 5

CONCLUSION

In this dissertation, a new matching theory called ordered element matching is rigorously proven using the theory of order statistics. Outlier elimination is also derived to improve the matching performance continuously. Based on these strategies, a new matching technique called "complete-folding" is developed to convert a mismatched unary-weighted array to a well matched binary-weighted array. In order to demonstrate the new matching technologies, a 15-bit binary-weighted current-steering DAC is designed and fabricated in a 130nm CMOS process. From the measurement results, both of the DAC's DNL and INL can be at the 15-bit accuracy level with a very small area.

Dealing with the increasingly large variability in nanometer and emerging processes is a fundamental challenge facing the whole semiconductor community. The knowledge and design strategies developed in this dissertation offer great potential for maintaining or improving precision and linearity performance of a large class of analog and mixed-signal circuits in the presence of large variability. Such advantage can be directly translated into a flexible tradeoff between smaller area and better matching performance. The dramatic system level matching improvement with a relatively low cost can benefit numerous matching-critical circuit designs in many electronic systems, which are often found in communications, computers, medical equipments and many other technology markets.

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The new matching strategies are applicable to all science and engineering problems in which accurate system level matching of a large array of mismatched components is desirable. It will inspire more researchers to apply statistical knowledge innovatively in the IC design areas for reliable, robust and high-performance operations in the variability-excessive processes.

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